

Industrial Instrumentation
Prof. Alok. Barua
Department of Electrical Engineering
Indian Institute of Technology – Kharagpur

Lecture - 23
Signal Conditioning Circuits - II

Welcome to the lesson 23 of Industrial Instrumentation. In this lesson, we will continue with the signal conditioning circuits. So, this is the signal conditioning circuit II. In lesson 22, we have discussed some signal conditioning circuits. We have discussed the filters and basically we concentrate on the signal amplifier filter. But, as you know that filter is one of the, one of the most vital part for analog signal processing, so we have devoted at least two, one and half lessons for filters. Now, these analog filters are off the shelf devices, I mean you can make the filters with a very low cost and it will give you good performance also if you can design it properly.

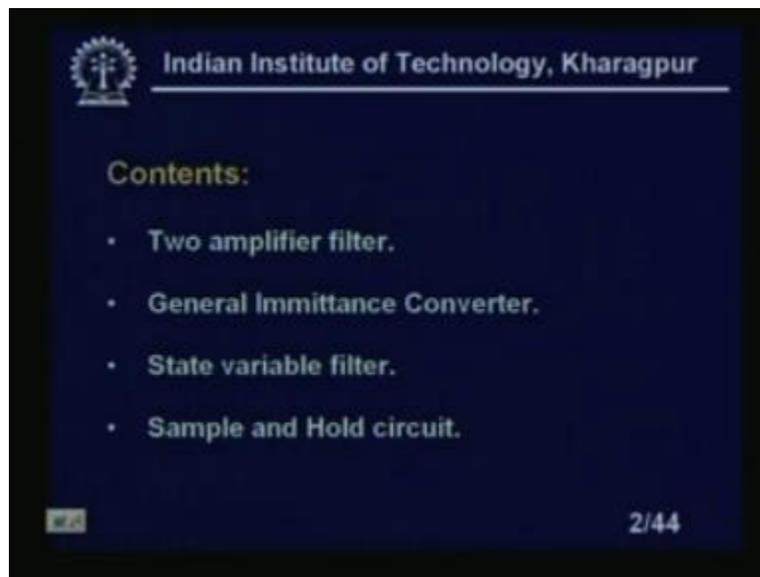
Now, the signal amplifier filter suffers from the drawback that the tuning of the filters is very difficult. As you know the filters has some typical parameters. This is ω_p , Q_p and K which we have discussed in the lesson 22 in details and these basically depends on some resistance and capacitance, right? Now the, in the case of filters, whatever the, you will design, whatever the filters you will design, obviously you need you know that you need perfections of the components, I mean if you say that the you have designed components, I mean actual design equation gives you a component value of 923 ohm, so instead of 923 ohm it is very difficult to get that value you may get it, little **deviate**, even if you get that exact value there will be some tolerances of that resistance which will give you, which will lead you to, ultimately once you design the circuits some sort of tuning of the I mean these filter parameters ω_p , Q_p , k , ω_z , Q_z .

Now, in the problem and the problem of the signal amplifier structure is that it is a low cost, its signal and dynamic range is also good. Its signal to noise ratio is also good. Unfortunately if you do not, if your technology does not permit very tight component tolerances, so the tuning of the filter parameter is very difficult in this case of filters and

in this lesson, lesson 23, 23, we actually discuss these two amplifiers and the general immittance converters, two amplifiers based general immittance converters, then two amplifier based filters and state variable filters and then sample and hold circuits and then logarithmic and antilogarithmic amplifier.

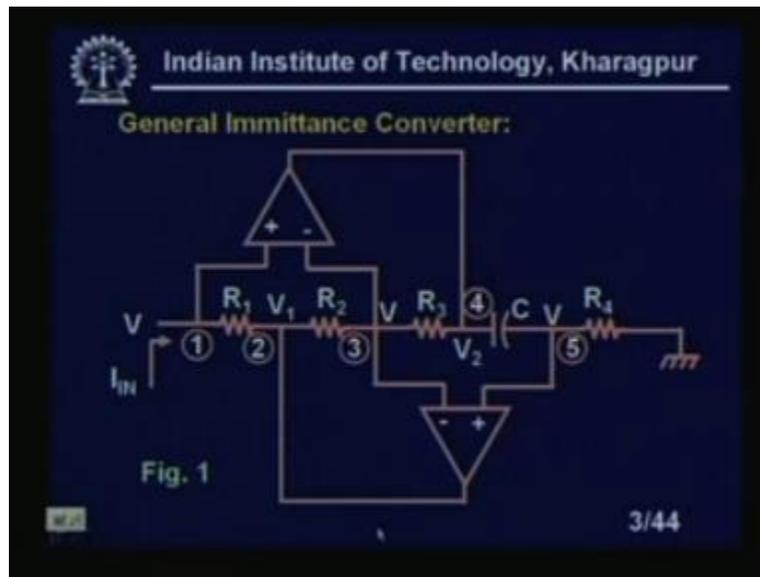
This is all, I mean this all is very common sort of, I mean, I mean circuits which is frequently used in signal processing of signal conditionings.

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Let us now lesson 23 you see, the contents of this lessons are two amplifier filters and general immittance converter and state variable filter, then we have sample and hold circuits.

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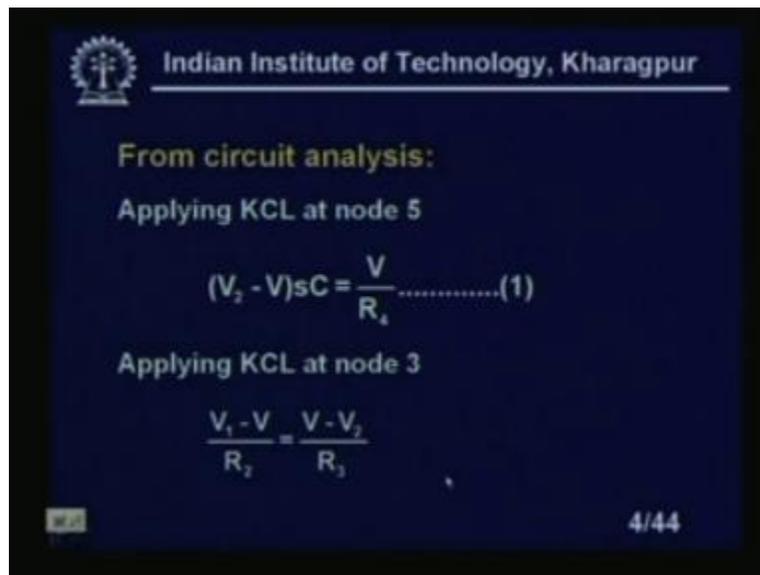
We will also, now let us look at the general immittance converter. You see, the general immittance converter, the circuit looks like this. You can see here that that in case suppose I am interested to measure the output, the input impedance of the circuits, so from this point what is the input impedance circuit? So, I assume that this voltage is V and obviously we can see here that you can see here that this resistance, I mean this is connected to ground and this general immittance converter is basically a device or circuit which will give you the, you can simulate inductance from the capacitance.

As you know the, it is very difficult to implement the inductance in integrated circuits. So, people tried over the years to simulate this inductance with the help of capacitance. Now, the general immittance converter, you can simulate inductance with the help of a capacitance; you can simulate capacitance with the help of inductance. But, nobody actually simulate capacitance with the help of inductance, because that is not necessary. In interior circuits we can always fabricate capacitance of the wide value, so widely different values in the chip itself, which is not possible in the case of, in a in the, if I want to do it, the inductor in the, in the chip. Even though people tried for last 2, 3 years to make a on chip inductance, but it is still in the research state, right?

Now, you see that I want to measure the input impedance or I want to look at the input impedance of the circuit, looking from this terminal, right? So that in this connector I have connected a voltage source V and I measure the current which is going inside, right? So, you see, two op-amps are connected. So that is the reason we call two amplifier structures and I mean, let us make the analysis of the circuits. We will apply the Kirchhoff's voltage. Now, it is, one thing is very common, you see. This op-amp has very high input impedance, right, so that this potential at the node 1 and potential at the node 3 is same.

Again, since the, this op-amp, this potential 3 is, node 3 is common, node 3 is common here, you see here, so this is connected to the, again the second amplifier. So, this potential, node 3 potential and node 5 potential is same, clear?

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So if I now, I apply the Kirchhoff voltage law in the node 5 we will get, if you apply the Kirchhoff for the circuit analysis, applying the KCL, Kirchhoff's current law I will get $V_2 - V$ s C equal to V by R_4 . Now, let us look at what is, so this is our V_2 . You see here this is our V_2 . So, this is our V_2 , this is our V_1 . Now, I want to apply, this is the, in this loop these are Kirchhoff's current law. Let us look at what will we get. This,

so applying Kirchoff's current law also at the node 3, we will get $V_1 - V$ by R_2 minus V by R_3 .

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Or,
$$\frac{V - V_1}{R_2} = \frac{V_2 - V}{R_3}$$

Substituting $(V_2 - V)$ from (1) we get

$$\frac{V - V_1}{R_2} = \frac{V}{sR_3R_4C} \dots\dots\dots(2)$$

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So, $(V - V_1) / R_2 = (V_2 - V) / R_3$. So, if this is the equation, so obviously substituting $(V_2 - V)$ from equation 1, we get $(V - V_1) / R_2 = V / (sR_3R_4C)$, right?

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Applying KCL at node 1

$$I_{in} = \frac{V - V_1}{R_1} = \frac{VR_2}{sR_3R_4C}$$

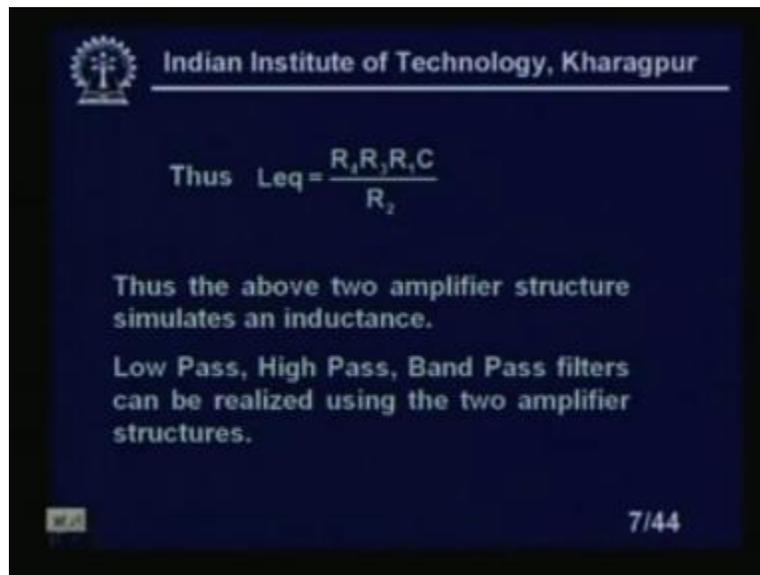
Or,
$$\frac{V}{I_{in}} = \frac{sR_3R_4C}{R_2}$$

Or,
$$Z_{in} = \frac{sR_3R_4C}{R_2} = sley$$

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So, applying KCL at node 1, I can write I_{IN} , that means current which is flowing inside just at the input node, $V \text{ minus } V_1 \text{ by } R_1 \text{ equal to } V \text{ by } R_2 \text{ by } s R_4 R_3 R_1 C$. So, obviously so $V \text{ by } I_{IN}$ or the input impedance of the circuit will look like $s R_4 R_3 R_1 C \text{ by } R_2$, right? So, Z_{IN} is equal to, the input impedance of the circuit at the node 1 can be written as $s R_4 R_3 R_1 C \text{ by } R_2$. Now you see, these entire things I can write as an equivalent inductance, you see this entire thing, is not it? So, I can write it sL eq. So, we can see, interestingly using one single capacitor I can simulate inductance in the circuits. So, I have used one capacitor and some resistors. So, I am uniting actually the inductance in the circuits, right? So, it has a tremendous impact in the signal processing, in instrumentation at least.

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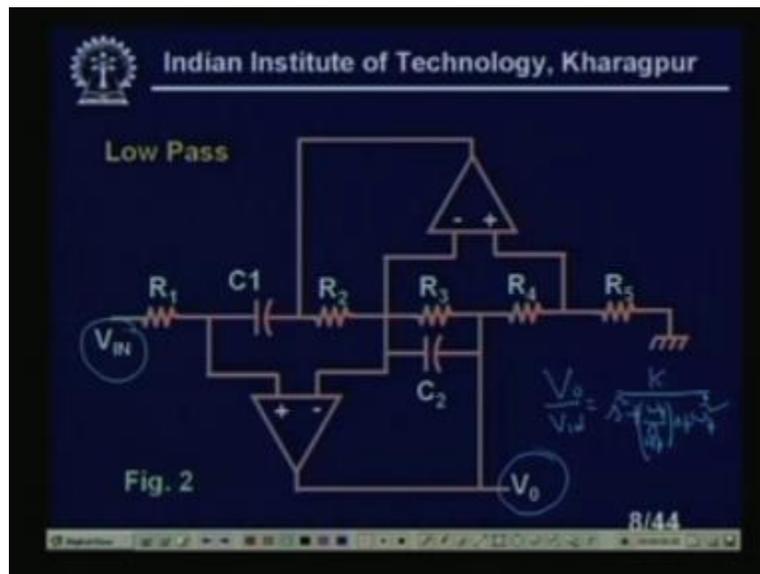


So, thus I can write the L equivalent or inductance equivalent equal to $R_4 R_3 R_1 C \text{ by } R_2$. You see there is a various combinations of these; you can have any one of this one. Suppose you can choose R_4 also as in, in, I mean capacitance by which you can, you can get the equivalent inductance, right? Now, thus the above two amplifier structure simulates an inductance Now you see, one thing is very important. If you look at this circuit, you see this particular circuit will generate actually the grounded inductance.

Now, if I want to generate, if I want to simulate the floating inductance, then these two circuits should be connected back to back, right? Only that time you will get the inductance, the floating inductance. Now, the inductance which we have generated here is the grounded inductance. Now, with the help of these inductances I can obviously simulate low pass, high pass, band pass filters can be realized using these two amplifier structures. I can realize low pass structures, I can realize high pass structure, I can realize band pass filters using the two amplifier structures.

Now you see, if you compare this single amplifier structures and two amplifier structure, you won't get much advantage in these two cases, except the, except in the form that that you will find that in the case if you use the band pass filter it will give you very high input impedance and resonance, which we will not get in the single amplifier structure. Otherwise all the problems what you have in the case of single amplifier structure that means the tuning difficulty which is most obvious in the case, in this case also will remain there. So, I am not getting an advantage compared to the single amplifier structure, so far the tuning of the filter is concerned, right?

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Now low pass filter, let us look at this low pass structures that means between input, this, between this input and this input, output I will get a low pass structure. That means V_O by V_{IN} will give you a value like, will give a value like K divided by s^2 plus ω_p by $Q_p s$ plus ω_p^2 and this type of structures it will get, right?

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From circuit analysis,

$$\frac{V_o}{V_{IN}}(s) = \frac{\frac{1}{R_1 R_2} \left[\frac{1}{R_4} + \frac{1}{R_5} \right] R_3}{s^2 + \frac{s}{R_3 C_2} + \frac{R_5}{R_1 R_2 R_4 C_1 C_2}}$$

K

$= \frac{1}{s} + \dots + \dots$

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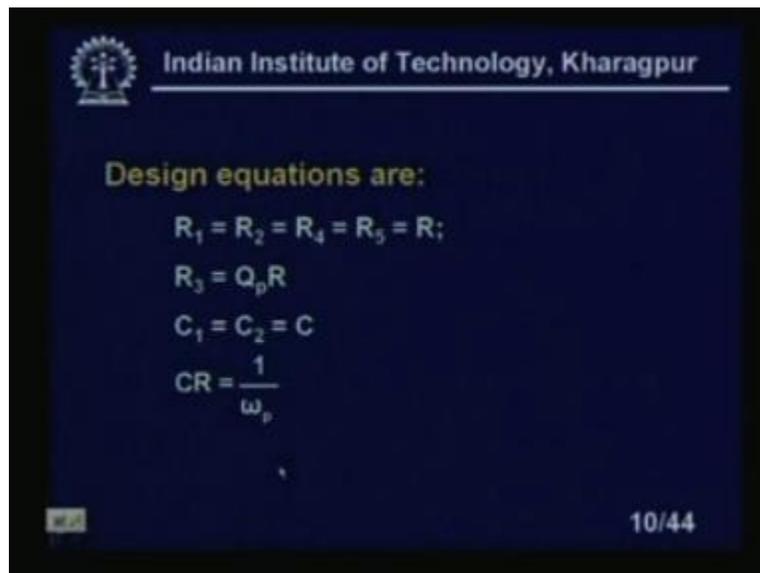
Now, if I want to, try to analyze this circuits, from circuit analysis I can find out that the V_O by V_{IN} is $\frac{1}{R_1 R_2} \left[\frac{1}{R_4} + \frac{1}{R_5} \right] R_3$ multiplied by $\frac{1}{R_4 + R_5}$ multiplied by $R_3 C_1 C_2$ and upon s^2 plus s by $R_3 C_2$ plus $\frac{R_5}{R_1 R_2 R_4 C_1 C_2}$, clear? Now see that, I mean I can, as, as it happened in the case of general immittance, I mean making the circuit analysis for the general immittance converter that same thing we can do it here also to find the overall, I mean transfer functions in the s domain of this circuit, right?

Now, also I can write the nodal matrix of this network and find the transfer functions. I am not going to details of that. Now, let us go back again. So, this is my circuit. So it is a very equal I mean I can, obviously this I can write, what I can write? This I can write K equal to as I have just written s^2 plus ω_p by $Q_p s$ plus ω_p^2 , is not it?

So, this will give you ω_p square. So, square root of this will give you the, square root of this will give you ω_p . See, if I make the square root of this, I will get the ω_p and this will give you ω_p by Q_p , right and this will give you capital K.

So, obviously what is, you can see also here it is very difficult, you see R_3 is present, obviously you can choose R_3 to tune the Q_p . So, it is not that difficult. You can choose R_3 to tune Q_p , but in, in tuning the K that means gain constant is also difficult, because you see whatever there R_1, R_2, R_4, R_5 , everything is present there. It is very difficult to tune the ω_p and capital K independently, though I can tune Q_p and ω_p independently in this particular type of circuits, right?

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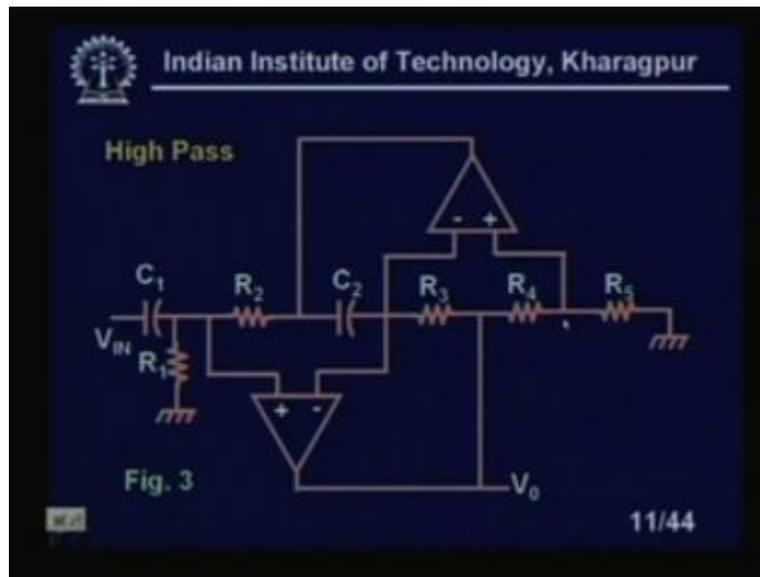
Design equations are:

$$R_1 = R_2 = R_4 = R_5 = R;$$
$$R_3 = Q_p R$$
$$C_1 = C_2 = C$$
$$CR = \frac{1}{\omega_p}$$

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So, design equations are R_1, R_2, R_4, R_5 equal to R , I have taken. R_3 equal to $Q_p R$ we have taken Q_p and C_1, C_2 all equal C . You can, all you can take 1 Farad, accordingly the resistance will come and C multiplied by R equal to 1 by ω_p . So, ω_p equal to 1 by CR .

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Now you see, the high pass filter slightly structure, the basic two amplifier structure remains the same. May be I am making little modification. You see this is basic two amplifier structure remains same. Again I am giving the input here, I am taking output from this position, right? You see, the two amplifier structures I am giving the input here, I am taking the output here. See here, as, as it happens in the case of general immittance converter, in this cases also I can, I can take the, transfer, find the transformation between an input and output and I can find, I can find the transfer functions as well as I can find the design equations for this type of high pass filters, right?

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From circuit analysis,

$$\frac{V_o}{V_{in}}(s) = \frac{s^2 \left[1 + \frac{R_4}{R_5} \right]}{s^2 + \frac{s}{R_1 C_1} + \frac{R_4}{R_2 R_3 R_5 C_1 C_2}}$$

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You see, from circuit analysis obviously I can write s^2 into $1 + \frac{R_4}{R_5} s^2$ plus $\frac{s}{R_1 C_1}$ plus $\frac{R_4}{R_2 R_3 R_5 C_1 C_2}$.

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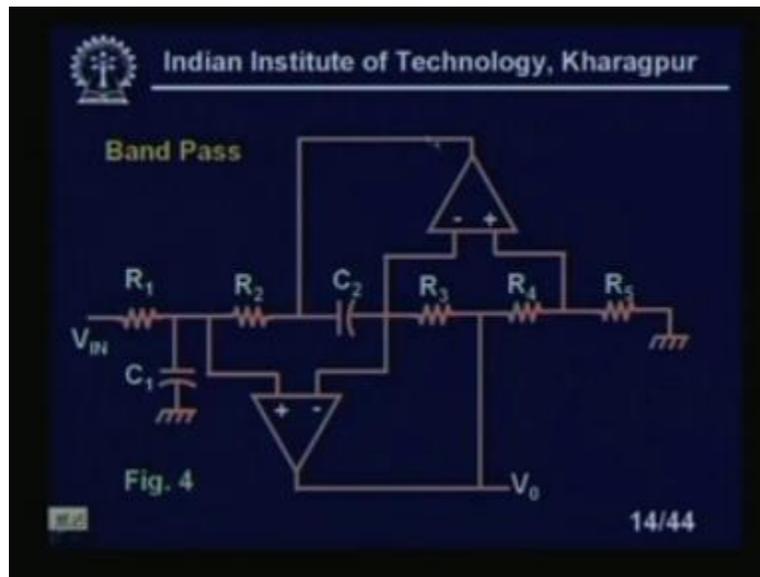
Design equations are:

$$R_1 = Q_p R$$
$$R_2 = R_3 = R_4 = R_5 = R$$
$$C_1 = C_2 = C$$
$$CR = \frac{1}{\omega_p}$$

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Now design equations are R_1 equal to $Q_p R$; R_2, R_3, R_4, R_5 equal to R . C_1, C_2 equal to C and CR equal to $1/\omega_p$, right?

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Now band pass cases you see here that R 1, similar structures only there is some difference at the input side. Again, I am giving the input here at this positions, so I am taking the output from this position. You see, I am giving the input in this position, I am taking the output from this position; input at this position, output at this position, fine. So, again I am finding the transfer function $V_{\text{out}} / V_{\text{in}}$ in s domain.

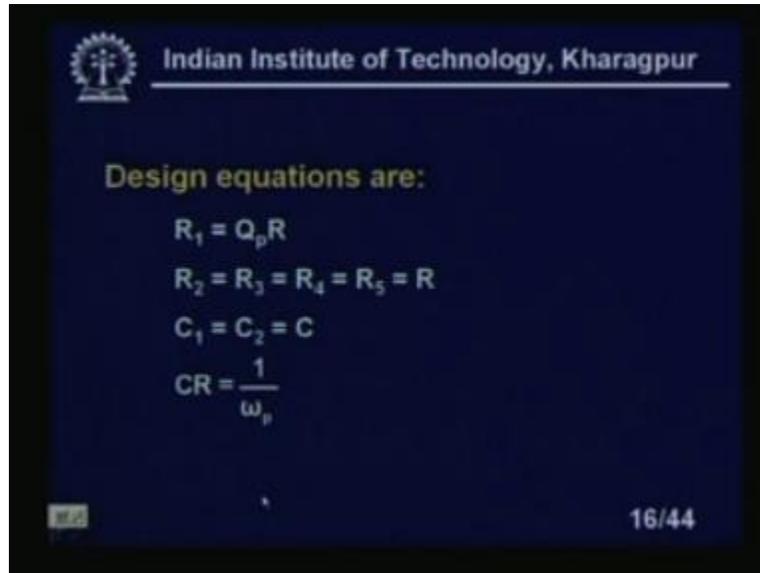
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From circuit analysis,

$$\frac{V_o}{V_{in}}(s) = \frac{s \left[1 + \frac{R_4}{R_3} \right] / C_1 R_1}{s^2 + \frac{s}{R_1 C_1} + \frac{R_4}{C_1 C_2 R_2 R_3 R_5}}$$

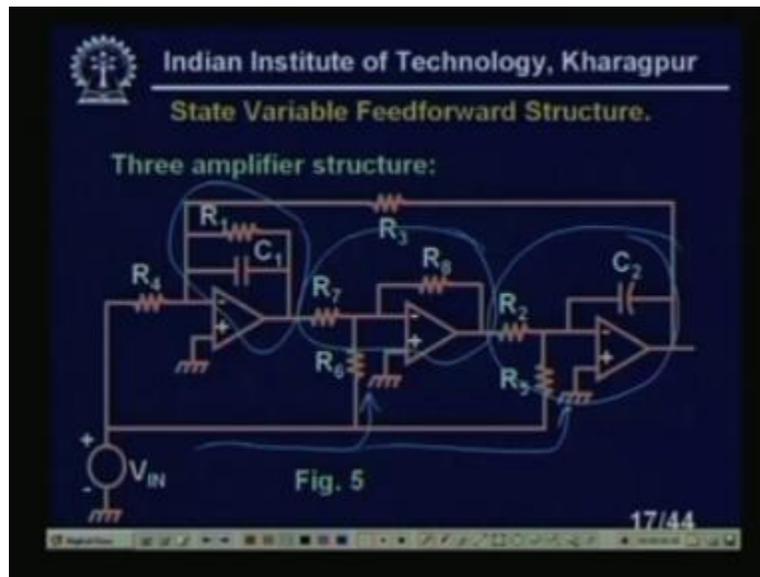
So, I will get a transfer function which looks like this. So, obviously it is a, you can see here there is a single zero at the origin and two complex conjugate poles. So, $V_{out}(s)$ by $V_{in}(s)$ equal to s $1 + \frac{R_4}{R_5} + \frac{C_1 R_1}{s^2} + \frac{s}{s^2 + s + \frac{R_1}{C_1} + \frac{R_4}{R_5}}$, right?

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The design equations looks like this R_1 equal to $Q_p R$; R_2, R_3, R_4, R_5 equal to R , C_1 equal to C_2 equal to C and CR equal to $1/\omega_p$.

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Now, state variable feed forward structure looks like this. Now you see I, we have discussed about the signal amplifier, signal amplifier structure using two amplifiers. I have just discussed only low pass, band pass, high pass, but you can use, you can simulate, you can generate other, I mean you can make the other topology like the high pass notch, low pass notch or band reject or low pass also with the signal amplifier structures, right? I am not going to details of that, so I am just giving the two amplifier structure, where we can make low pass, high pass, band pass. Please remember, but please remember, you can generate other filter functions like high pass notch, band pass notch, band reject, as well as all pass structure by this two amplifier topology.

Now, as it happen, as I told you that in the case of signal amplifier structure, it is just impossible to tune orthogonally all the filter parameters. In the case of two amplifier structures we have seen that we can independently tune the ω_p and Q_p , quite obviously but I cannot tune Q_p , ω_p and K independently. So to, people need some other structure, where we can make total orthogonal tuning of the filters, right? So, that type of structure is basically state variable feed forward structure, let us look at.

The three amplifier structure looks, you see that we need three amplifiers. Why it is calling feed forward? You see, there is a feedback. There is no doubt this is a state variable structure. I have a **lossy** integrator. You see what is this actually? This is a **lossy** integrator, right? This is an inverter, simple inverter and this is another integrator, is not it? So the, first one is a lossy integrator or damped integrator. Then you have an inverter, then we have again another integrator and you see here there are feed forward through R 6 and R 7, because input is coming here, it is going to R 4 to the first amplifier, then through R 6, you see through R 6 and through R 5 we are giving to feed forward.

This type of structure can generate any filter functions. We will see that is advantage of this type of structure, tremendous advantage of this type of I mean structure. It is, it is available in the cheap form also, this type of filters, National semiconductor makes this filter. It is called universal filter, where you can have, so one or two elements outside which you can tune to get your desired value of omega p and Q p, right?

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From circuit analysis we get

$$T(s) = \frac{-R_8}{R_1} \left[\frac{s^2 + s \left(\frac{1}{R_1 C_1} + \frac{1}{R_4 C_1} + \frac{R_5}{R_7} \right) + \frac{R_5}{R_7 R_2 R_3 C_1 C_2}}{s^2 + s \left[\frac{1}{R_1 C_1} \right] + \frac{R_5}{R_7} \left[\frac{1}{R_2 R_3 C_1 C_2} \right]} \right]$$

Handwritten form: $T(s) = -k \frac{s^2 + cs + d}{s^2 + as + b}$

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Now, design equation looks like this. From a circuit analysis we get, we have to, we can make the circuit analysis, we can say that R, R 8, minus R 8 by R 6 s square plus s 1 by R 1 C 1 1 by R 4 C 1 R 6 R 7 R 6 by R 7 1 upon R 3 R 4 C 1 C 2 s square plus s 1 upon R 1

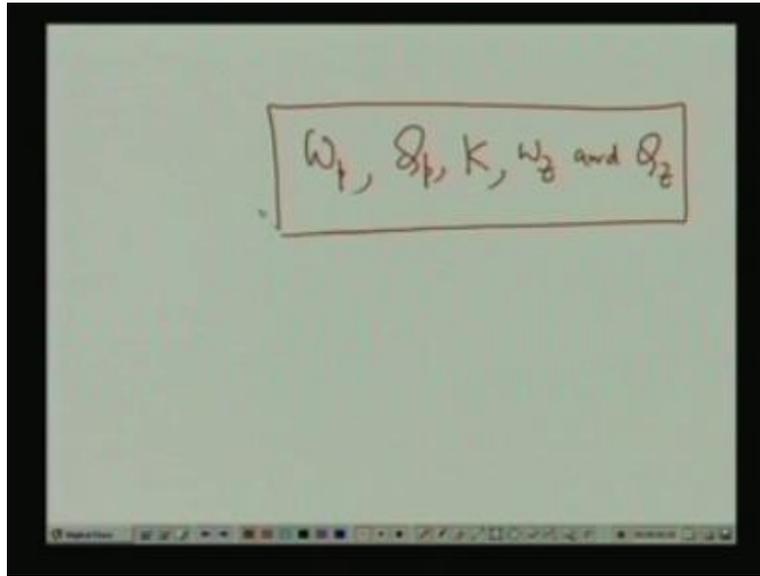
$C_1 R_8$ by R_7 upon $R_2 R_3 C_1 C_2$, right? One thing you see here, it is very important, you see here that this is very similar to the structure, I can write $T(s)$ equal to $\frac{K(s^2 + d s + c)}{s^2 + a s + b}$, is not it; very similar to this type of structure.

Now, for this reason you can see this, all this value, R_8 , these components, you can see this component, this one, so we can realize by some resistance and capacitances. So, if I purposefully make that portion zero, obviously I can integrate it. Suppose in this case, suppose if I make c zero and d zero so it will be high pass structure, right? Similarly if I make, suppose R_6 infinite, in that case it will be a, your, I can make this as a low pass or, or band pass structure; like that it goes, right? So, with this type of structure, obviously I can generate any filter function.

Only problem, if you look at the numerator you see that here we have a subtractive term at the, as the coefficient of s . So, the problem with this subtractive term is that it will, we have to make a signal, we are getting the, we are making it zero, this coefficient zero by signal subtractions, right? So, in that type of situation what will happen you know, if there is a , if there is, suppose in that case, if suppose during cancelation, if this coefficient is not exactly zero, this coefficient is not exactly zero, then what will, this coefficient is not exactly zero, then we will find that even though I tried to realize the low pass structure, so the, in the case of low pass structure as you know the pole zero pattern will be like this one.

So, two complex conjugate poles and no zeros, so it will find that it will not exactly the same pole zero pattern, right? So, this is the only difficulties in that this type of state variable structures. Otherwise it is a tremendous advantage. Its, its sensitivity is also quite low. Its tuning is a great advantage. You can see in the next slide I can show you what are the different elements we can choose to tune ω_p , Q_p , ω_z , Q_z independently, right?

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Because as you know, in that, I mean in the filter parameters we, always we know that we have to tune omega p. I can take another pen. Omega p, Q p, capital K, omega z and Q z, these are the things, I mean which we are going to simulate, right? So, I mean this, the, the parameters which you have to tune it with some resistance elements, capacitance, we will not use for tuning. Now, how I can make, now orthogonal tuning means that if I use some resistance to tune or some capacitance I will consider the resistance, if I consider some resistance, suppose this omega p I am, want to change or modify or tune, so other, by changing some resistance if I tune omega p, other filter parameters should remain intact. That is called the orthogonal tuning.

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From circuit analysis we get

$$T(s) = \frac{-R_2}{R_6} \frac{\left[s^2 + s \left(\frac{1}{R_1 C_1} + \frac{1}{R_4 C_1} + \frac{R_4}{R_7} \right) + \frac{R_4}{R_7 R_3 R_5 C_1 C_2} \right]}{\left[s^2 + s \left(\frac{1}{R_1 C_1} \right) + \frac{R_4}{R_7} \left(\frac{1}{R_2 R_3 C_1 C_2} \right) \right]}$$

Handwritten notes:

$$T(s) = -k \frac{s^2 + cs + d}{s^2 + as + b}$$

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Now, if you go back, you see here, you see here what will happen? In this case I can choose some of the resistance. Suppose if I choose some of the resistance to tune omega p by that time what will happen? You see that if I choose some resistance to tune omega p is, there is omega p, what will happen that omega z, Q z may change. It does not matter, let it go wherever it goes. Then we will use some other resistance or capacitance to bring it back to the original position, right? So, let us look at that.

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The above can also be written as

$$T(s) = K \frac{(s^2 + cs + d)}{(s^2 + as + b)}$$

The design equations are:

$$C_1 = C_2 = 1$$

$$R_2 = R_3 = R_7 = R_4 = R_5 = R = \frac{1}{\sqrt{b}}$$

$$R_1 = \frac{1}{a}, \quad R_6 = \frac{1}{K(a-c)}, \quad R_8 = \frac{\sqrt{b}}{Kd}, \quad R_9 = \frac{1}{K\sqrt{b}}$$

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Now above equations, as you can, can also be written as $T(s) = K \frac{s^2 + cs + d}{s^2 + as + b}$ and the design equations are $C_1 C_2 = 1$, $R_2 R_3 R_7 R_8 = 1$, $R_1 = 1$ by \sqrt{b} and $R_4 = 1$ by a , $R_5 = 1$ by \sqrt{b} and $R_6 = 1$ by K .

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The design equations mentioned above yield positive element values for $a \geq c$.

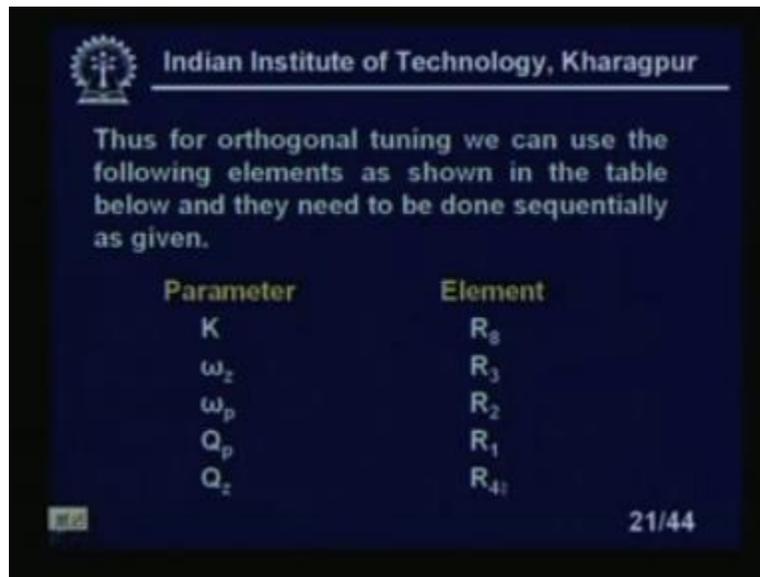
The above equation can also be written as

$$T(s) = K \frac{s^2 + \left(\frac{\omega_z}{Q_z}\right)s + \omega_z^2}{s^2 + \left(\frac{\omega_p}{Q_p}\right)s + \omega_p^2}$$

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The design equations mentioned above yield positive element values for a greater than c. This, most of the cases this will be satisfied, a will be greater than c. This equation, design equations mentioned above yield positive element values for a greater than c and the above equations can also be written as $T(s) = K \frac{s^2 + \omega_z/Q_z s + \omega_z^2}{s^2 + \omega_p/Q_p s + \omega_p^2}$.

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Thus for orthogonal tuning we can use the following elements as shown in the table below and they need to be done sequentially as given.

Parameter	Element
K	R_8
ω_z	R_3
ω_p	R_2
Q_p	R_1
Q_z	R_4

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Thus, for orthogonal tuning we can use the following elements as shown in the table below and they need to be done sequentially as given. You cannot haphazard fashions. These are the filter parameters and which particular element, passive elements we will choose to tune it, let us look at. For capital K, gain constant I am tuning R_8 , right? For ω_z , I am using R_3 . For ω_p , I am choosing R_2 . ω_p Q_p equal to R_1 , I am choosing R_1 to tune and Q_z equal to R_4 , this completes the tuning of the, all the filter elements. You have to go in particular this sequence that otherwise there will be a problem.

You see, because if you choose, tune R_8 , let us look at I am taking examples of tuning R_8 or R_3 ; ω_z K for R_8 and ω_z equal to R_3 , let us look at.

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From circuit analysis we get

$$T(s) = \frac{-R_8}{R_6} \frac{\left[s^2 + s \left[\frac{1}{R_1 C_1} + \frac{1}{R_4 C_1} + \frac{R_8}{R_7} \right] + \frac{R_8}{R_7} \frac{1}{R_2 R_3 C_1 C_2} \right]}{\left[s^2 + s \left[\frac{1}{R_1 C_1} \right] + \frac{R_8}{R_7} \left[\frac{1}{R_2 R_3 C_1 C_2} \right] \right]}$$

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Now you see here, so K we are using R_8 and ω_z R_3 . Let us look at, you see that K , R_8 is changing. I am getting the proper value of R_8 by tuning the, this proper, proper value of capital K . This is the, because this K is equal to R_8 by R_6 , is not it? So, I am tuning R_8 to getting proper value of K , but you look at that R_8 is also present in the expressions of ω_p . So, ω_p will change, right? It does not matter, let it change. So, I will bring it back by using some other elements to its desired value.

Similarly, you see that when I am, after K , once the K is tuned, now I am choosing R_3 to tune ω_z . What is ω_z here? You see it is ω_z . Now, this will also vary. By that, during that time it does not matter, I will choose some other elements later on, so to tune the, get the ω_p exact desired value. So, this sequence, that is the reason I am telling that particular sequence you have to maintain, otherwise there will be a problem. Now you see, so once I have chosen, I have chosen R_3 to tune ω_z , I am not using R_3 anywhere to choose any other further elements. I will choose some other elements to tune the ω_p or Q_p like that, right? So, that is the case that I want to explain to you.

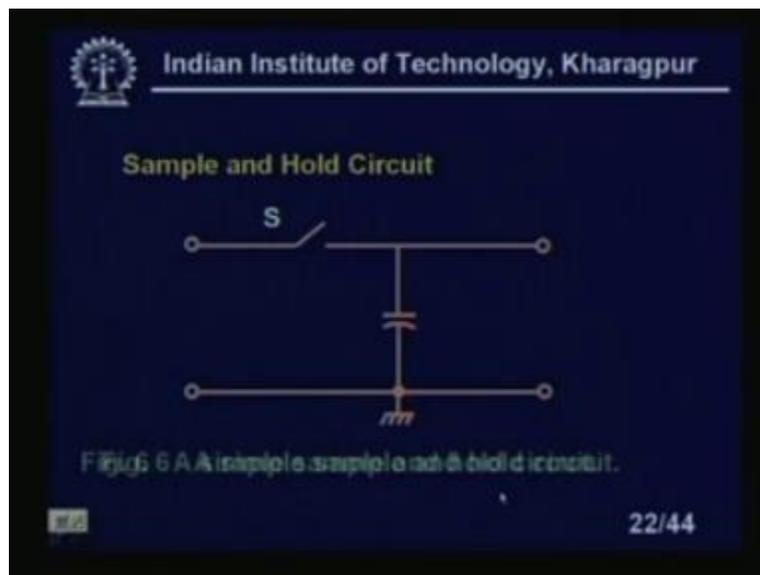
You see it is here, sorry, here you see ω_z R_3 ω_p R_2 Q_p R_1 , so if I vary ω_z , then what will happen? You see if I vary R_3 ω_z , ω_p will vary. It does

not matter, I will use R_2 to bring it back to the original value, right or desired values. Similarly, I can tune Q_p and Q_z by R_1 and R_4 respectively, right? This ends the particular, the only, the filters. That means we have discussed in the lesson 22, the signal amplifier structures. Then in the lesson 23 we have discussed the two amplifier structures, we have discussed the three amplifier state variable structures.

State variable structure has another advantage. It is, I mean it is the frequencies, it is the sensitivities, logarithmic sensitivity is very, very low. Though the one single problem with the signal amplifier structures is the power dissipation and also the dynamic range of the filter, because as you know, if you are increasing the number of op-amps you are making the, your signal to noise ratio poorer and poorer, right? But, I mean since it has the advantage of the tuning and it has the advantage of the low sensitivity, this structure is preferred over the other signal amplifier to the two amplifier structures.

Now, let us go back to sample and hold circuits. Let us look at that.

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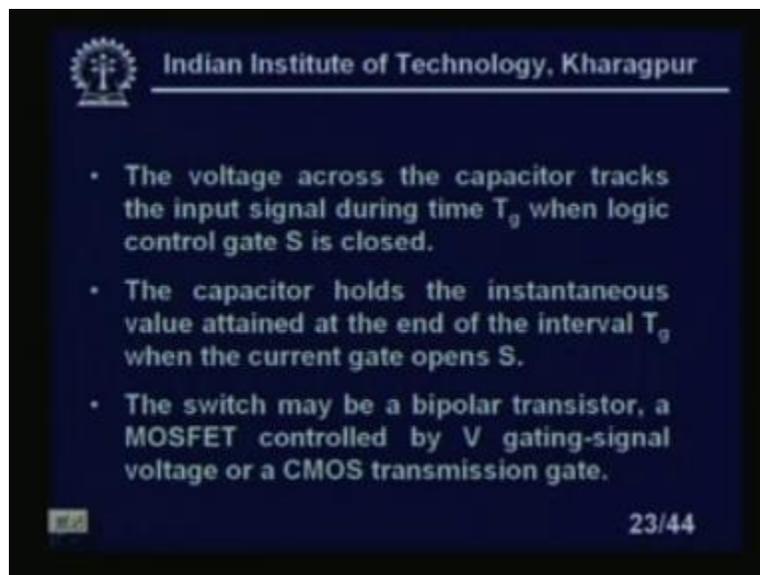


You see, this is a simple sample and hold circuit. In sample and hold circuits it is very much necessary in many signal condition. One of the good examples of the sample hold

circuit is a DC. Now, analog to digital converters we have, you know there are various types of analog to digital converters. We have successive approximations analog to digital converters, we have the counter, we have dual slope adc, we have a flash adc, there are so many adc's are there, enhanced dual slope adc.

Now, all these cases I assume that during the conversion whatever small it may be, all the, all the adc has some conversion time, we are assuming that the, during the conversion the signal remains stationary of value. Its value is not changing that is to be assured by the sample and hold circuits, right? So, sample and this is one of the simplest form of the schematic of the sample and hold circuit. This is a switch and we have a capacitor here. When I close the switch, the, it is charged, the capacitor, the capacitor is charged by the input voltage and when I open it, it will hold for that for some period, right, whatever small it may be. So, during that times I can make my conversion, my conversion complete; let us look at, sorry.

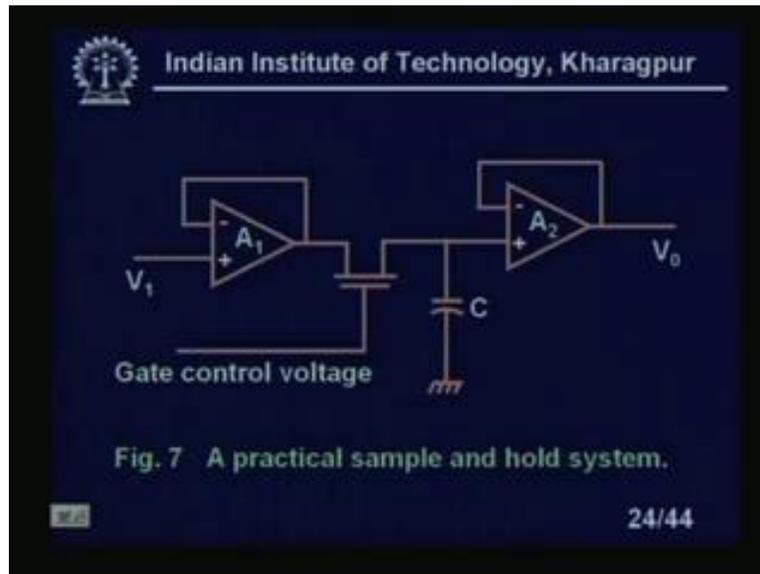
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Now, voltage across the capacitor tracks the input signal during the time T_g , when the logic control gate S is closed. This is a logic control gate. I can use some MOS gates also, right, for this purpose. The capacitor holds the instantaneous value attained at the end of

the interval T_g when the current gate opens S , right, fine. So, during T_g , so it holds the charge. The switch may be a bipolar transistors or a MOSFET controlled by V gating the signal voltage or a CMOS transmission gates.

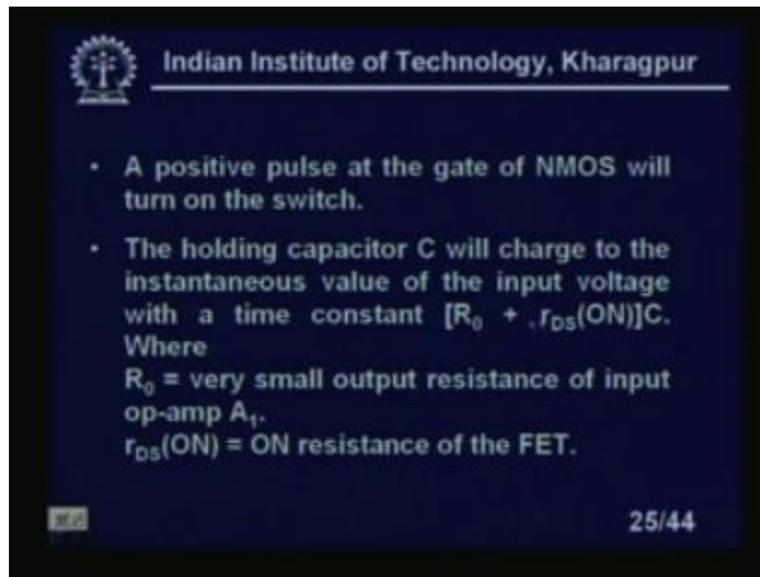
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Now as you see, this is an example. So, I am using one, I mean MOS gate. Here I am using one buffer amplifier at the input side, another buffer amplifier at the output side, right? So, this **gates**, this analog signals, so whenever this gate voltage if it is NPN, suppose if it is a MOSFET, I mean MOSFET, if it is the signal is like this, what will happen? So, whenever this voltage is positive it is open. So, whatever the charge it has, voltage has, it will be, come to this and capacitor will be charged to that voltage.

Once this gate voltage is removed, so that voltage is supposed to stay here. So, during that time if the V_1 change and that will not affect this output voltage or the voltage on the capacitor C . That is the basic theory of the sample and hold circuit.

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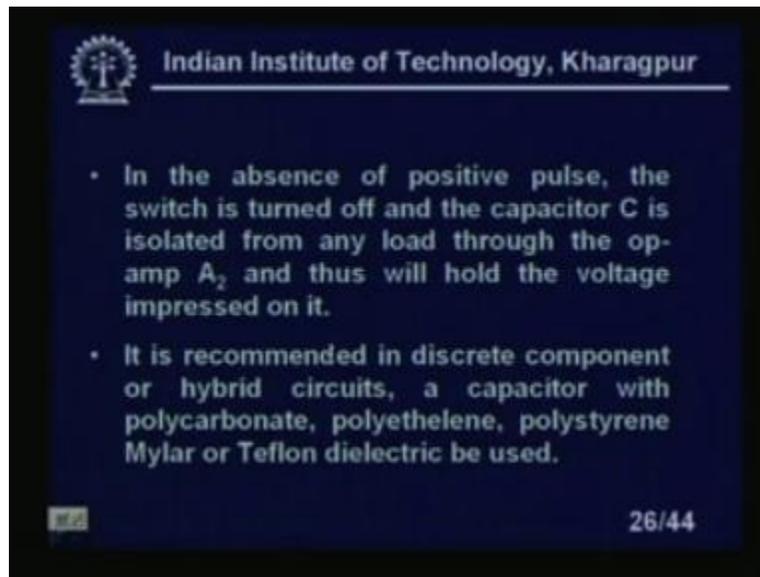
- A positive pulse at the gate of NMOS will turn on the switch.
- The holding capacitor C will charge to the instantaneous value of the input voltage with a time constant $[R_0 + r_{DS(ON)}]C$.
Where
 R_0 = very small output resistance of input op-amp A_1 .
 $r_{DS(ON)}$ = ON resistance of the FET.

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Now, positive pulse at the gate of NMOS if I assume it is NMOS, so in the gate I have to give positive pulse, positive signals or control voltage. If I use a PMOS I have to give negative voltage or negative signal at the gate of the NMOS or of the PMOS. The hold capacitor, holding capacitor C will charge to the instantaneous value of the input voltage with a time constant of R_0 plus $r_{DS(ON)}$ multiplied by C. You know the time constant is basically R into C, so where R_0 is very small output resistance of the input op-amp A_1 . Assume that the output obviously this op-amp has a very low output impedance.

Now $r_{DS(ON)}$ is ON resistance of the MOSFET; I am writing FET is the MOSFET, ON resistance of the MOSFET, right?

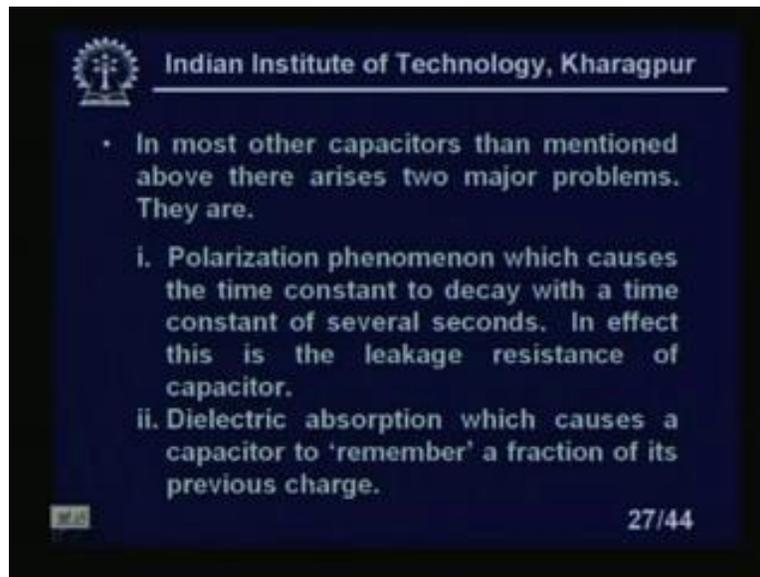
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In the absence of the positive pulses, the switch is turned off and the capacitor is isolated from any load through the op-amp A 2 and thus will hold the voltage impressed on it. So, because there is an output capacitance, obviously it will isolate the, our utput circuits, this sample and hold circuits will be totally isolated from the, I mean subsequent circuits which follows after the, which follows the amplifier A 2, right? So, this charge will be hold, because there is no path to discharge, so that charge should hold, if there is no leakage in the, obviously in the capacitor. So, the capacitor is the crux or the heart of this sample and hold circuits. We will discuss what are the different types of capacitors typically used for making a sample and hold circuits?

It is recommended in discrete component or hybrid circuits a capacitor with a polycarbonate, polyethylene, polystyrene, Mylar or Teflon dielectrics be used. This is because all these names actually came for the capacitors for the typical dielectric. This is, dielectric switch is used for the, which is placed inside the plates or a parallel plate capacitors. So, we are talking of the, not necessarily it will be parallel but it can be, I mean foil type also that as it happened in the case of electrolytic capacitors.

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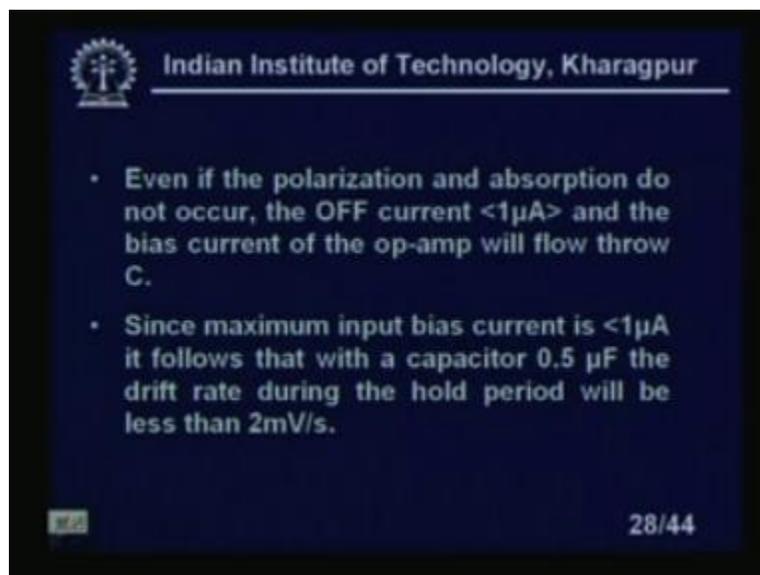
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- In most other capacitors than mentioned above there arises two major problems. They are.
 - i. Polarization phenomenon which causes the time constant to decay with a time constant of several seconds. In effect this is the leakage resistance of capacitor.
 - ii. Dielectric absorption which causes a capacitor to 'remember' a fraction of its previous charge.

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In most other capacitor than mentioned above, there, there arises two major problems. They are polarization phenomenon which causes the time constant to decay with a time constant of the several seconds. In effect this is the leakage resistance of the capacitor. Dielectric absorption which causes a capacitor to remember a fraction of its previous charge that also creates the problem.

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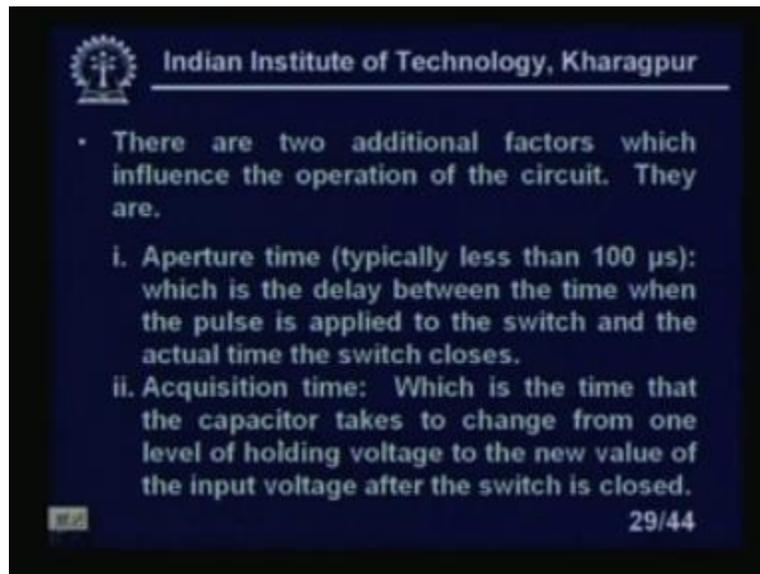
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- Even if the polarization and absorption do not occur, the OFF current $<1\mu\text{A}>$ and the bias current of the op-amp will flow through C.
- Since maximum input bias current is $<1\mu\text{A}>$ it follows that with a capacitor $0.5\ \mu\text{F}$ the drift rate during the hold period will be less than 2mV/s .

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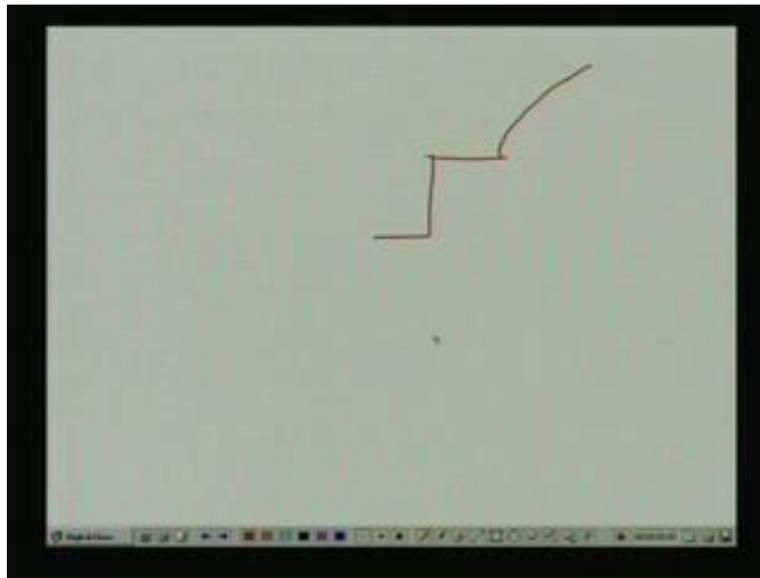
Even if the polarizations and absorption do not occur, the OFF current or the, I mean current of the switch is less than 1 micro ampere less than and, and the bias current of the op-amp will flow through the capacitor C, right? That is the problem. Since maximum input voltage, input bias current is less than 1 micro ampere it follows that with a capacitor .5 micro Farad the drift rate during the hold period will be less than 2 millivolt per second.

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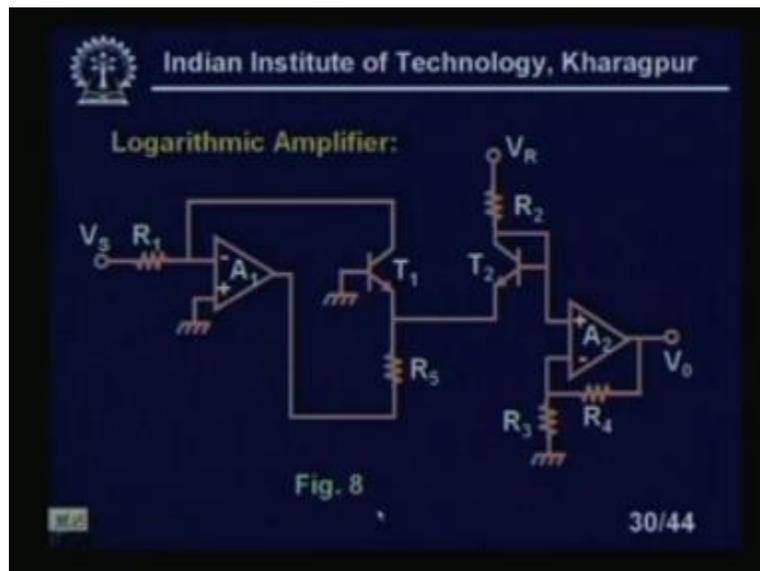
There are two additional factors which influence the operations of the circuit. They are the aperture time typically less than 100 micro second which is delay between the time when the pulse is applied to the switch and the actual time the switch closes. Aperture time typically less than 100 micro second which is the delay between the time when the pulse is applied to the switch and the actual time the switch closes. Acquisition time which is a time that the capacitor takes to change from one level to holding voltage to the new value of the input voltage after the switch is closed, is not it?

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Because you see what will happens that is capacitor, suppose I have some voltage, I have some voltage on the capacitors, so we should charge it. Suppose its voltage is changing, so it will from this place for during that it remains constant, so it will go again to that value, we are talking about that. Acquisition time which is the time that the capacitor takes to change from one level of holding voltage to the new value of the input voltage after the switch is closed.

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Now, next we will discuss the logarithmic amplifier. Logarithmic amplifier is basically an amplifier which will give the signal the output, this one. So, the output should be some constant multiplied by logarithmic of the voltage V_s that is the function of the logarithmic amplifier, right? So, the output is a logarithmic of the voltage V_s . This is the basic principle of logarithmic amplifiers. We can use two transistors and two amplifiers to make the logarithmic amplifier. The circuit analysis shows that is basically used, these, the diode characteristics of the, because you know diode characteristics is exponential characteristics of the voltage current relations of the diodes that means we will utilize to make these logarithmic amplifiers.

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Assuming
 $i_{B1} \ll i_{C1}$ and $i_{B2} \ll i_{C2}$

We get

$$V_o = -V_t \left(\frac{R_3 + R_4}{R_3} \right) \left[\ln \frac{V_s R_2}{R_1 V_R} \right]$$

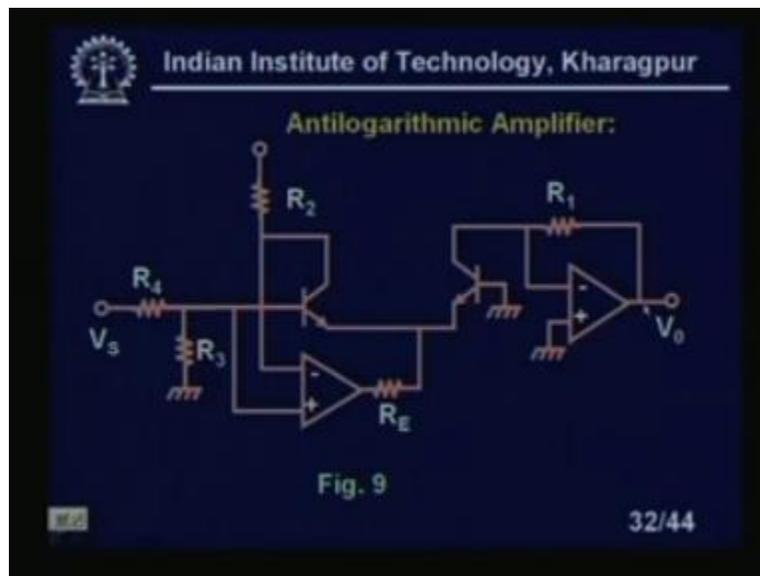
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If I make the circuit analysis you see here assuming that i_{B1} is less than, than less, much, much less than i_{C1} that is quite obvious in all the cases of the transistors and in the transistor 2 also i_{B2} base current is much, much less than the collector current, in the transistor 1 the base current is much, much less than collector current, in base two, transistor 2, base current is much, much less than collector current, we get V_o equal to minus $V_t \frac{R_3 + R_4}{R_3} \ln \frac{V_s R_2}{R_1 V_R}$. So, obviously you can see that if I assume this $R_1 R_2 V_R$ are all constant, so only variable here is the

V_s , because V_t is also constant, but for a particular room temperature this V_t will also remain constant.

So, you can see that V_{naught} if I assume this $R_1 R_2 V_R$ reference voltage all are constant, so the, this output voltage is, is a logarithmic of the voltage V_s which we have impressed, right, which we have applied at the input of the circuit. So, this is basically the logarithmic amplifier. Similarly, since we have a logarithmic amplifier we can have antilogarithmic amplifier also, let us look at.

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So, an anti-logarithmic amplifier circuit looks like, this is basically same. You can see two transistors and two amplifiers A 1 and A 2 and two resistance R 4 and R 3 at the initial side. So, V_s output will be, output will be antilogarithmic of the voltage which you are giving here.

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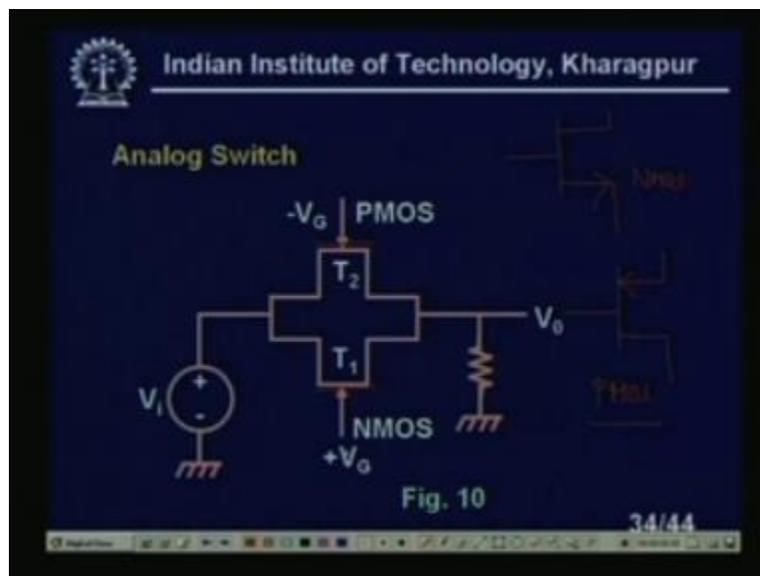
Here

$$V_o = \frac{R_1 V_R}{R_2} \exp\left\{\frac{-V_s - \frac{R_3}{R_3 + R_4}}{V_T}\right\}$$

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So, let us if you make the circuit analysis I can write that V_o equal to R_1 into V_R by R_2 exponential of minus V_s V_T into R_3 R_3 plus R_4 , right? So we can see this one, this is a negative logarithmic of the, so this is a, obviously this is, you can see this is a antilogarithmic amplifier.

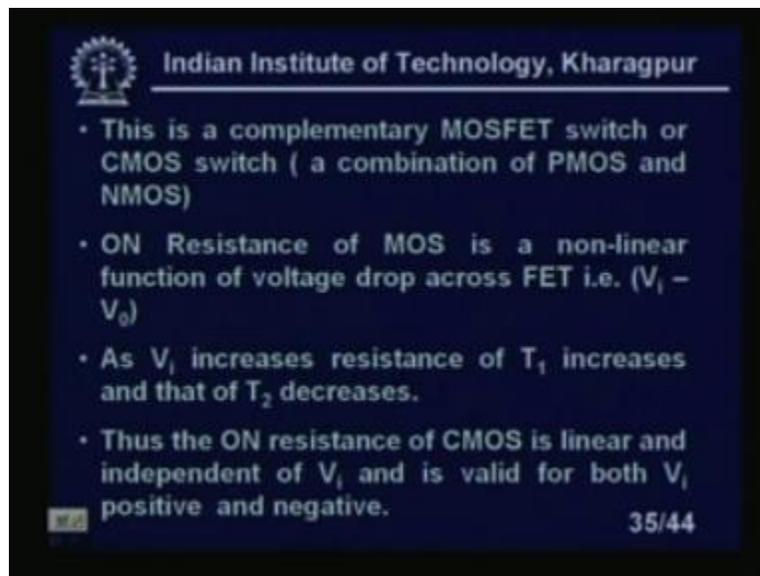
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Now, analog switch is extremely used in signal conditioning circuits. Analog switches are the two switches one NMOS and one PMOS. I think this figures I have to modify. Actually it looks like this and this is, this, this is NMOS, this is PMOS or I can use the symbol like this as it happened in the case. This is NMOS and in the case of PMOS there is no arrow or you can write like this one, right? This is in the case of PMOS. I am not showing the substrate, so here bulk and now the, if you look at this NMOS PMOS these all basically called a CMOS switch. It is extensively used in the signal conditioning circuitry in the multiplexing, in demultiplexing.

Now what is this PMOS? Why should I use two MOS in parallel? Because if have to give plus V_g here I have to give minus V_g here to turn on these two transistors.

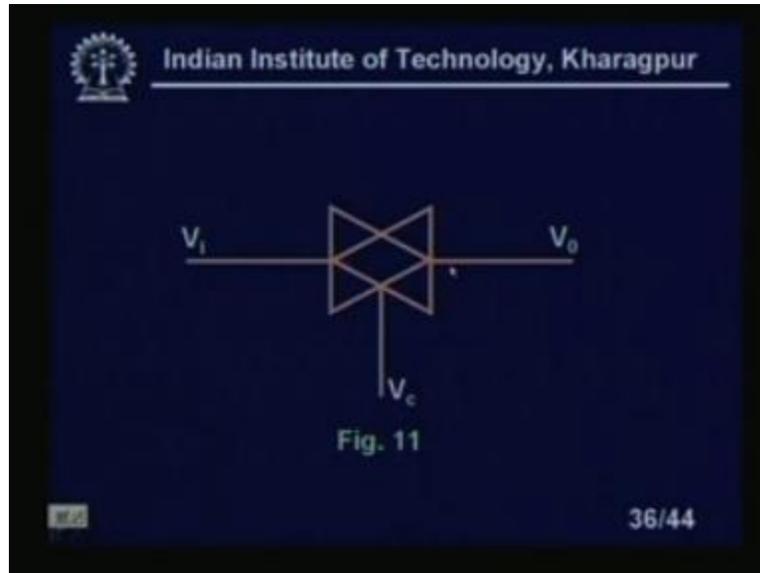
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There are some advantages. You see this is a complementary MOSFET switch or CMOS switch, a combination of PMOS and NMOS in parallel, right? Now, ON resistance of the MOS is a non-linear function of the voltage drop across FET. That means V_i minus V_0 , so the non-linear function of the FET. So, this can be linearized by using in one case it is increasing with the voltage, in another case it is decreasing with the voltage. If I use two MOS op-amp in parallel, so this will be nullified and the voltage relations, voltage and or

turn ON resistance relations will be perfectly linear or it will remain, sorry, I should, it should remain constant. So, as V_i increase resistance of T 1 increases and that of the T 2 decreases. Thus the ON resistance of the CMOS is linear and is independent of V_i and is valid for both V_i positive and V_i negative, right?

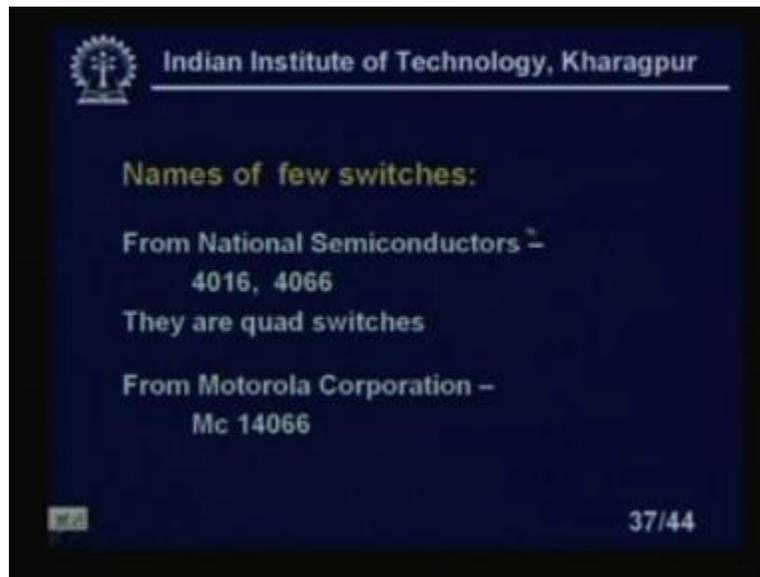
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Now, this is the symbol of analog switch. You can see this is a bidirectional analog switch. We have V_i , we have V_o and there is a control signal. This, when this signal is ON that means this is the signal MOSFET is turned ON. So, whatever the signal, analog signal that will appear at the output. This is, please note this is not an inverter switch or anything; it is analog switch. So, whatever the signal voltage here, whatever is the level of the voltage, it does not matter, if this signal is ON that signal will appear at the output. If you remove this signal V_c , so whatever the signal it does not matter that will not appear at the output of the analog switches.

Now, using this analog switch I can use a multiplexor and demultiplexing. Let us look at that.

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Names of the, there are some commercial, excuse me, there are some commercial analog switches. These are National semiconductor switches 4016, 4066. These are all quad switches, I mean four switches in one chip, right and from Motorola we have 14066. This is also the quad switches and that means one for, so it should be, it is a 14 pin DIP; in both the cases 14 pin dual inline package, right? In one case we will find that the, in each cases we will find there are, three pins is necessary - one for input, another for output, another for control. So, 12 switches done, so 2 more switches one for V SS, another one for V DD. So, it is 14 pin DIP which analog switches, right? So, both the National semiconductor, Motorola specifications we have given.

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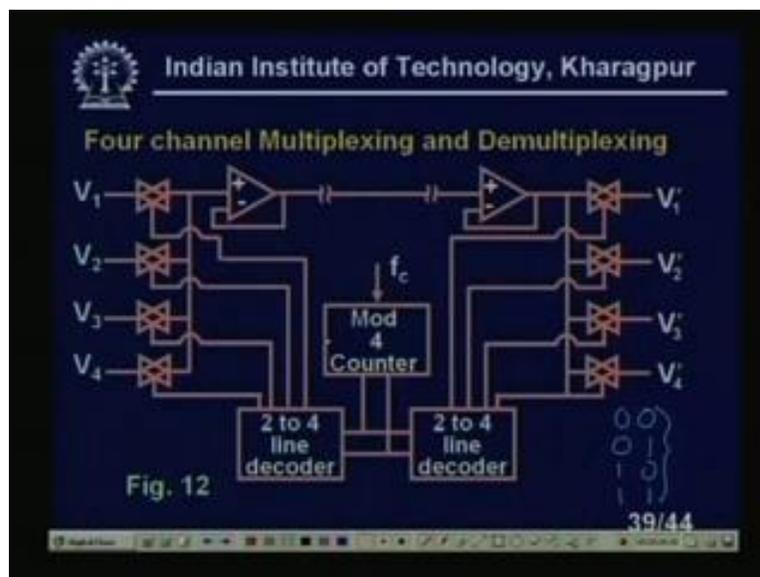
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- It is Bidirectional Analog Switch.
- A 14 pin DIP.
 - There are 4 switches on one switch.
 - 1 V_{DD} and 1 V_{SS} lines.
- ON resistance of the chip/analog switch is 100 Ω to 600 Ω .
- Input signals must lie between V_{DD} and V_{SS} where $V_{DD} = +5V$ and $V_{SS} = -5V$.

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Now, it is a bidirectional analog switch. It is a 14 pin DIP. There are four switches on one switch. These all are the specifications, one V_{DD} and one V_{SS} line. ON resistance of the chip, analog, I mean switch is around 100 ohm to 600 ohm. This value is little low, I mean you can keep, nowadays it is even less. So, input signal lie between V_{DD} and V_{SS} , where V_{DD} plus volt and V_{SS} will be minus 5 volt.

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Now you see, this is a one of the typical example of the multiplexing and demultiplexing. Now you see what is the need of multiplexing and demultiplexing? Now, basically this multiplexing demultiplexing is necessary to reduce the number of cables and also the number of hardwares. Now all of you know, most of you are using the calculators. In the calculators we have, nowadays as we can have afford, you can have a 10 digit display, you can have a 12 digit display, all those things.

Now it will be surprising to know, you always from, if you have a BCD signals, BCD signals you have to convert to the, I mean display. So, I need BCD to seven segment decoder. Now, my BCD's signal, BCD chip should be the same, same as the display unit. But, I can use a single decoder BCD to seven digit segment decoder to convert the signal to the seven segment display. This it can be very conveniently do if you can scan the signals, if you can multiplex and due to persistence of visions if you look at the calculator, it is we never seen that it is, it is not blinking, is not it? Due to persistence of vision it appears that it is constant. It is not flickering. Actually it is flickering that means one digit at a time they are displaying on the, on the display board, right?

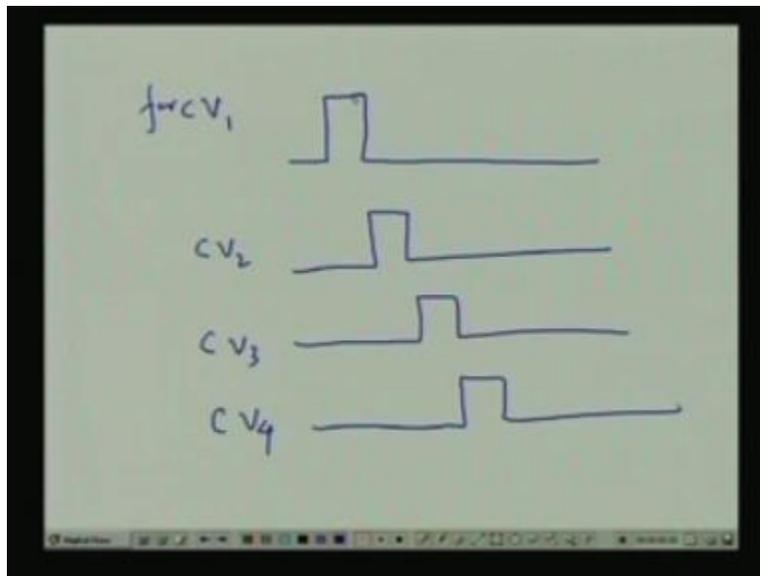
Similarly in the case of, suppose in the case of ADC we have also multiplexing. Demultiplexing, one of the good examples of this, this type of ADC is 0809. In 0809 ADC you will find it is a basically eight bit ADC. Now it has an input. I can, I can connect eight different input to this ADC. Even though ADC is more, only one ADC, inside the chip, but I can take the signals from eight different sensors. I can, from eight different thermocouples or eight different RTD I can take the signals, because it is multiplexing that signals one at a time and every time it is only one A to D converter converting the signals. Similarly I need one demultiplexor at the output also. All these thing is necessary to reduce the number of cables.

This is very important because the cable cost is a lot, because especially if you use a low capacitance cable I mean sorry, I mean, I mean where the capacitance capacity loss is less we will find that it is very expensive, right? So, to avoid that I always used multiplexing and demultiplexing; let us look at that. You see here this is basically analog

switches; four analog switches are there. You can see here I have analog switches. These are all analog switch. You can see this analogs, bidirectional analogs, so inputs are coming V 1, V 2, V 3, V 4 and we have a control signal one. This is, these are all control signals which is going here, right and we have a buffer amplifier. At the input we have buffer amplifier.

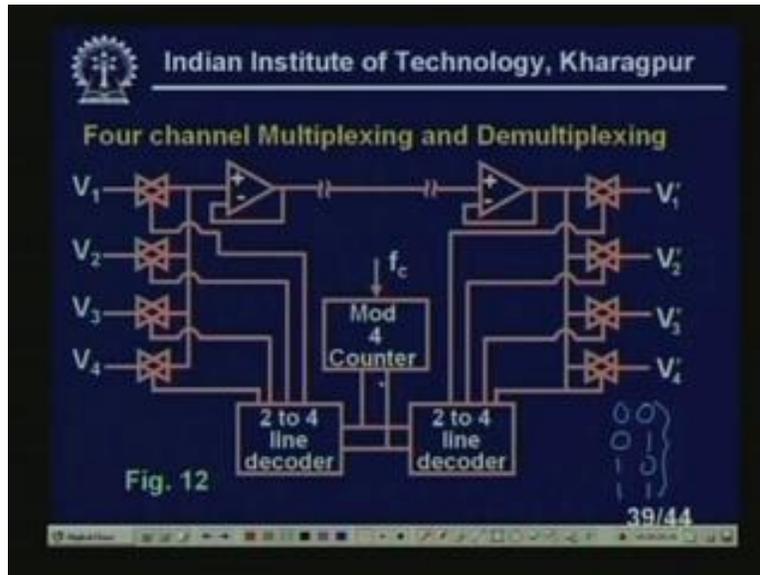
We have drawn broken lines, lines might be very long it is a data lines and you see what we are doing here. I need a two to four line decoders. What is the two to four line decoders? Only one line will be selected at a time. When this line, this switch will be selected all other switch will be deactivated during that time. This is very, it is not very difficult.

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You see I can have a, this type of signals. I can have a signals like this, you see here. So, this is the switch. This is V 1, for V 1 I should say or control V 1. This is control V 2, control V 3, control V 4. You see, when this is ON, only when, when this is high, only the switch 1, analog switch 1 will be selected all other will be deactivated, right? So, if we have a **shift** like this one, quite obviously I can achieve this type of signals.

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What is that? You see that when I am giving V_1 , control signal to V_1 which I have shown just right now, so all the signals, all the, even the signals are present at the input that will not come to the output, because you see the, all the outputs are connected together; all the outputs are connected. So it is, suppose that whenever this signal is ON, when this switch is ON all other switch will be deactivated. That means the signal will not come. So, it will be coming through this network. It is, again it is demultiplexed the outputs. So, V_1 will appear as a V_1 dash, V_2 will appear as V_2 dash, so and such sort of sampling I am doing here. So, similarly when V_2 will be ON, what will happen you see, this will be deactivated. So, this is connected at the input of the op-amp like this one. So, we have 2 to 4 line decoder here; you see we have 2 to 4 line decoder.

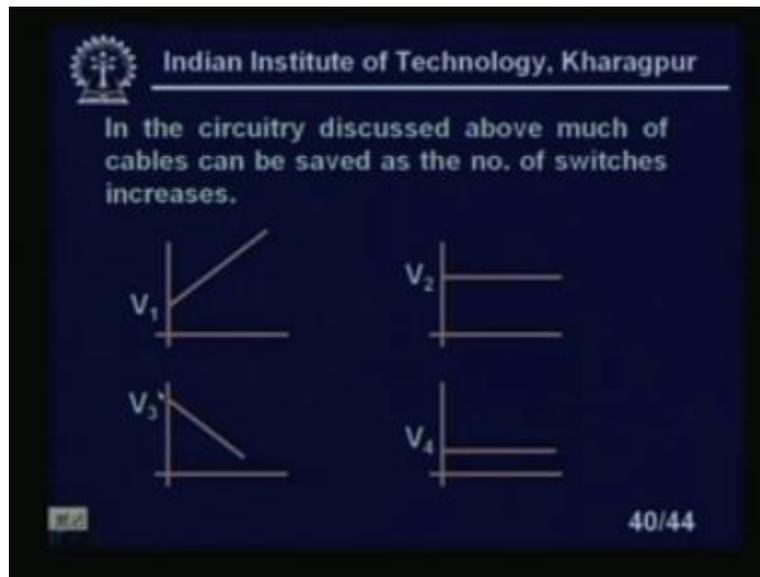
So, what is the function of 2 to 4 line decoder? So, we have a 2 bits signal, because in the 2 bits signal what are the different states I can have? You know, I can have 0 1, 0 0. I can take this one, I can have 0 0, 0 1, 1 0 sorry, I have 0 0, 0 1, 1 0, 1 1. This is the signals of 2 to 4 line decoders, because mod 4 counter have 4 different states. Since I have four lines, I need mod four counter. So, after 1 1, again it will go to 0 0. When 0 0 will be activated, so 2 to 4 line decoder. This is very simple. I can do with, with, with AND gate. So, this gate will be selected, so and all other gates will be deactivated. When this is ON,

so this will be OFF, right and when this is, when 0 1 will be there, so V 2 will be, this signal will be selected, when 1 0 will be there this signal will selected, when 1 1 will be there this signal will be selected, right? Same signal should go to the output also, right? So, this is the basically 2 to 4 line decoder

Now, one question that immediately arises then what is the use of this type of circuits? You see that if I do not use any multiplexing demultiplexing what will happen? I have a four signals V 1, V 2, V 3, V 4 that will be transmitted. So, four lines I need, but I need lot of hardware. You see the, so what actually I did? I achieved that I have saved only one line. In addition I need so many counters, decoders, all those things, right? So, counter it is necessary, decoder is necessary. I can manage with one decoder that is fine. I can just with, from the output of the decoder to go to the both the input and output that is not a problem, right?

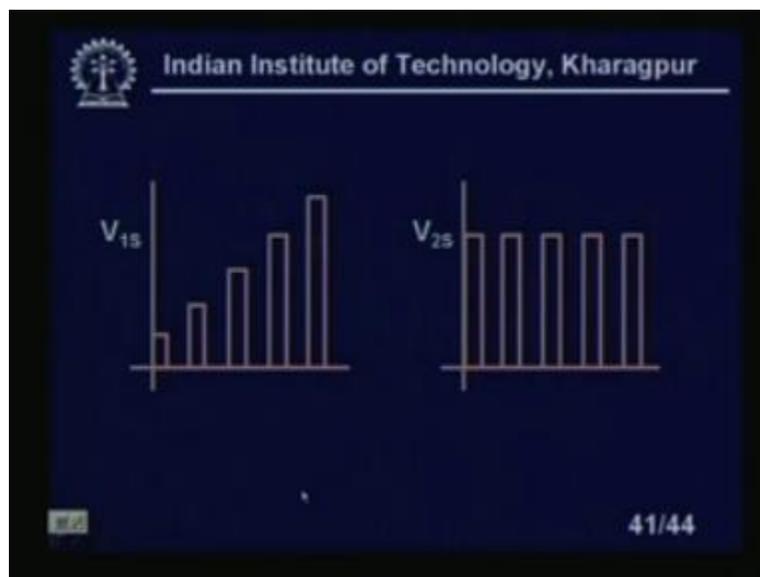
Now the question where, where is the saving? Saving will be there if the number of lines are more. If suppose if I have 12 lines, I mean 12 different sensors, in that case how many lines is necessary? If I have 12 different sensors, I need four lines for this one and one lines, five lines. So, I am saving seven lines. In that case seven cables, I am in that case. So, that is the advantage of the multiplexing and demultiplexing, right? So, people always, but you know that we have to, one to one synchronization should be there. That means when these lines will be selected, so simultaneous this line also should be selected during that. It is a not very difficult, because same pulse, same mod four counter output is coming to the both the decoder. So, when this will be selected, this will be selected and at that time all these three analog switch will be deactivated, This analog switches also will be deactivated. When this switch is selected this switch also will be selected, like that it will go, right?

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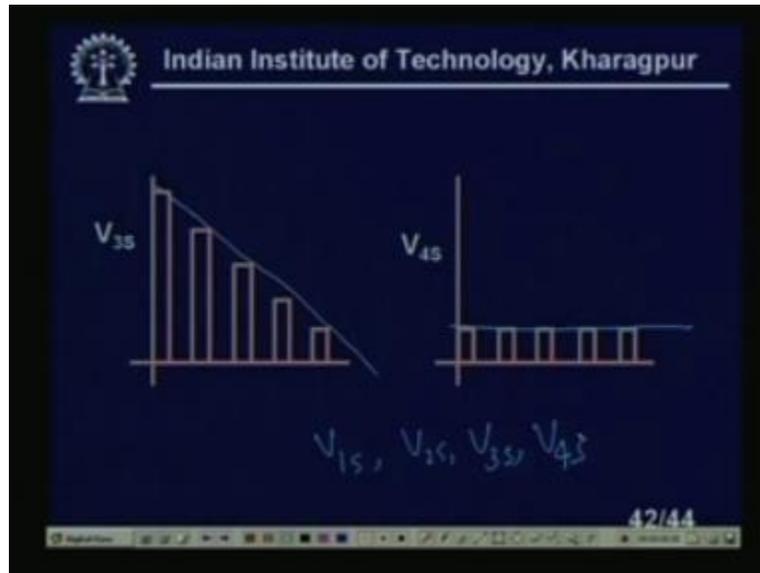
So, in the circuitry discussed above much of the cables can be saved in the, the, as the number of switches increases. Now you see that I am giving some inputs signal V_1 of different varieties of the signal V_1 , V_2 switches, slowly varying with time, increasing with time which is not varying with time. Now, if I sample this and some signal V_3 which is coming down and V_4 is also less value it is constant.

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See, if the signal looks like this one what is the sampled signal? Sampled signal should look like this one. This signal will not change.

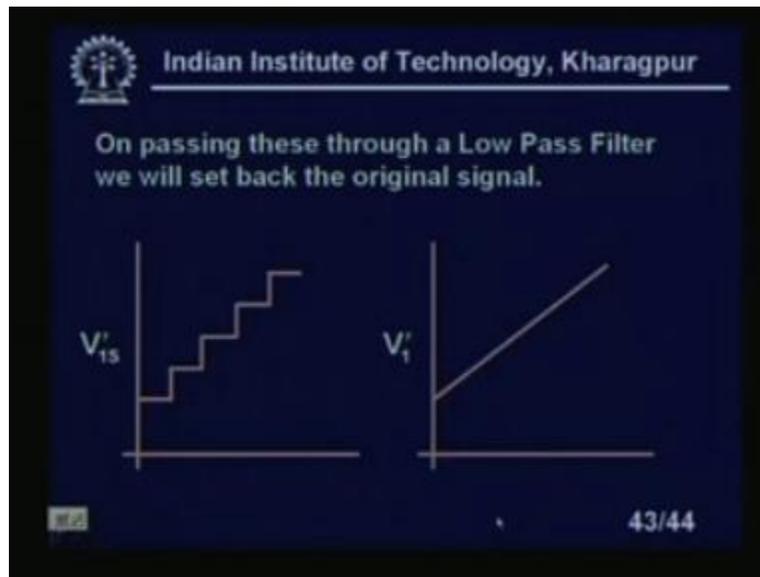
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Now this signals this is coming like this, this is coming like this. Now, what will happen actually? You see that if I pass this signal, how will you retrieve the original? My original signal does not look like this, is not it? How does my original signal look like? My original signal look like this, original signal look like this. So, this signal that mean V_{1s} , V_{2s} , V_{3s} , V_{4s} should pass through a low pass filter. If I pass this signal through a low pass filter, so obviously what will happen? This, all these things will go out. Actually I will get a good output which is very close to the input signals.

So, I can use a simple RC filter also at the, RC low pass filter at the output of the, output of the multiplexors. That means at, at this point you see here I can use some output signals. I can use some capacitors also, so which will reduce that high frequency components, so I will get a signals which is very similar to the input signals I have, which I have given here V_1 , V_2 , V_3 , V_4 , clear? So, this is the advantage of our multiplexing and you can see here, so if I pass this signal through a low pass filter, obviously I will get the original signal.

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Now, on passing these through a low pass filters we will set back the original signals that is quite obvious that I can get the original signal. So, obviously you can see the same type of hardware is also used in the case of display, digital displays where they are, we are saving the seven segment decoder, because that is a great saving. Even though those are in LSI, large scale integration, so the saving is there that with a single decoder I can and due to persistence of vision here also, see in many, in many cases I do not need sampling that fast, right? I do not have to monitor the temperature. Suppose I have a 100 thermocouples, I do not need to, I mean monitor the thermocouple temperature every minute, something like that.

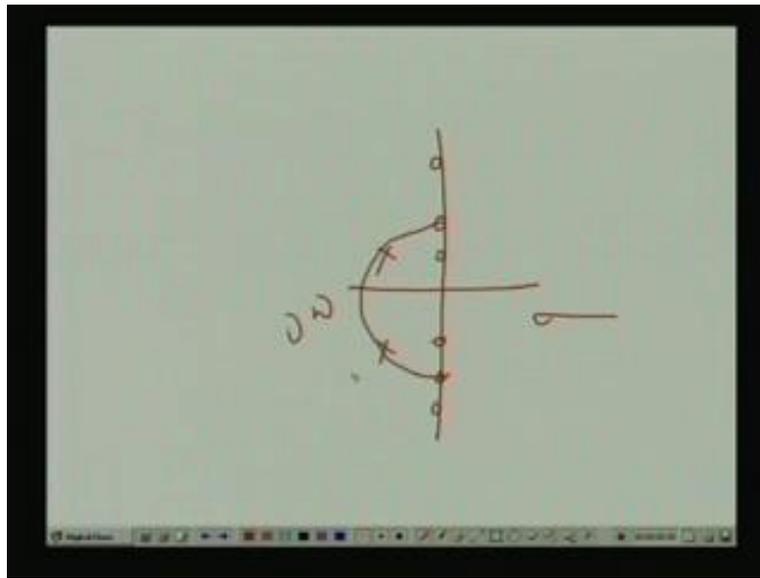
I can sample, suppose if I want in a 5 minutes that is more than enough. So, in that case accordingly I can make the circuit so that which will give you the, I can, I can sample the circuit like that. So, this is the advantage that in that case what I will do that I will save the, basically the hardware which is necessary to, I save the hardware which is necessary, I mean which, which is the great, which will reduce the cost of the entire systems or entire equipment. So, that is the advantage of the multiplexing and demultiplexing, whereas in the case of filter switch you have seen that is at the very beginning of the lessons we have discussed, you see the basically general emitter converter or inductance

simulators, sometimes it is called the inductance simulators, there are various types of name.

We call inductance simulators or gyrators. That means by using a capacitance I can use an inductance, by using an inductance I can use a capacitance. As I told you, nobody is simulate, I mean nobody simulate the capacitance with the help of inductance, but it is quite obvious people always try to simulate inductance with the help of capacitance, because having a real capacitance, real inductance in the circuit is very difficult. It is neither it is possible so far as for today to get a large value of the inductance and also we can have a, I mean if we want to do the simulation I can have a floating inductance as well as a we have a grounded inductance that means two grounded inductance if we connect back to back, I will get a floating inductance of the simulator, floating inductance circuits. So, these are the things which we have discussed.

We have also discussed the signal amplifier structures. During the lesson 22, we have discussed the two amplifier structures in the lesson and we have discussed also the, I mean two amplifiers as well as three amplifier state variable. Now, state variable structure is very attractive. Two amplifier structure has no advantage, additional advantage except that in the band pass cases it keeps the very high, very high input impedance. Only problem with the state variable structures we have seen that that because you see that the high pass structures, high pass, high pass or high pass notch or low pass notch, this type of filter functions is achieved by making the, the coefficients of s in the numerator zero and we have seen that that is actually done by the signal subtractions. So, if due to mismatching of the any resistance or capacitance it does not make zero that creates the problem.

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That means in the case of, as you know in the case of notch circuits as you know that we have always you know what will happen the, if you look at this is sigma j omega plane. We have a complex conjugate poles in the case and either I can have a zero here or I can have a zero here, here or here, here. Now, if it does not cancel that means there is no real part of the zeros, so that is only possible if the s part that means coefficient of s in the numerator is, is absolutely is zero, otherwise there will be no real part.

Now what will happen if the real part remains due if, if due to signal subtraction it is, it is not compressed, what will happen you will find that it will remain. So, this will be shifted to little bit on this side, so that will create the problem. So, the pole zero location will not be same, not exactly what is desired and also by, by that the exact notch functions may not be achieved. That is the only drawback. But nowadays as you know, the signal conditioning, the component tolerances are less and less going to be so that it is very easy to get the, whatever that is the value of the or what are the, whatever the design value of the resistance or capacitance that we can achieve very easily. So, with this we can come to end of the, so you see that is how does the signal comes so that I can staircase wave forms. So, with this I come to the end of the lesson 23 of Industrial Instrumentation.

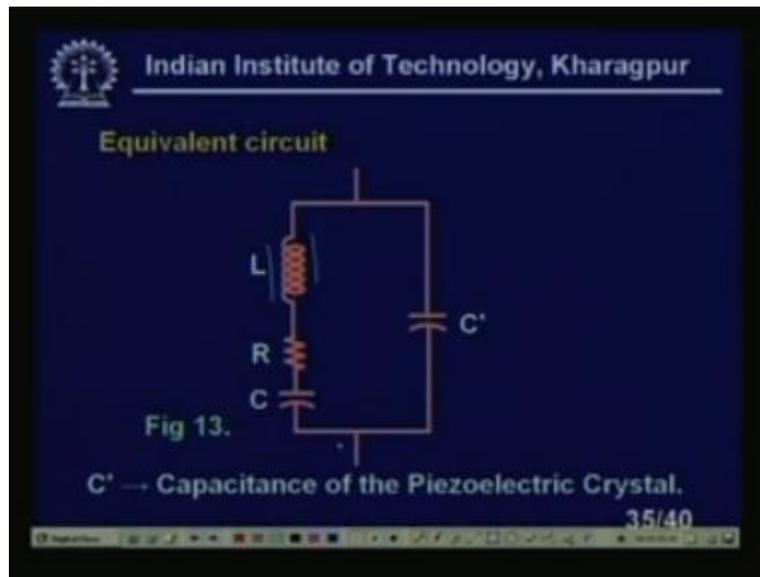
Preview of next lecture:

Welcome to the lesson 24 of Industrial Instrumentation. In this lesson we will consider piezoelectric sensors. Now, as you know piezoelectric sensors is based on piezoelectric crystals, right? So the, it has a property that if you apply a force across the surface of this piezoelectric crystals I will get a voltage and this process is reversible. That means if I apply the voltage I will get the force also. So, utilizing these principles obviously I can make the sensors which can measure force and piezoelectric crystals is extensively used for, as I told you that is reversible that is it is extensively used for generations of the ultrasonic waves.

As you know that the ultrasonic sensors are, are, is used, ultrasonic sensors are used extensively in the case of flow measurements and all these things like ultrasonic flow meters are there. So the, you have seen that actually there we are using the, to launch the ultrasonic signals, I, we want that ultrasonics, I mean piezoelectric sensors, piezoelectric crystals actually we have used there, so it is another use. Also, the piezoelectric crystals as you know it is used for measurements of, for the generation of the very stabilized frequency, because it is, piezoelectric crystal if you, we will see later on that it has, if you draw the equivalent circuit that you will find that it has a very high selectivity.

It helps to make the, make the oscillator which is very stable in frequency. These are the all different applications of the piezoelectric sensors. So, we will discuss one by one what are that and piezoelectric crystals we will find that I, I need a, a special type of amplifier to those, to amplify the charge generated across the plates of the piezoelectric crystals.

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The equivalent circuit is like this one. You see, I have an inductance. Let us look at, I have an inductance L . Then I have an inductance L , I have a resistance R , C and also a parallel capacitance C' . This value of L is very, very high in the case of piezoelectric crystals. That makes the frequency stability excellent otherwise nobody should care for these quartz crystals, right?

So, in this lesson we will see that at the first part of the lesson we have discussed the, basically the piezoelectric sensors which is used for the measurements of the displacements, accelerations, ultrasonic and which can be used as the ultrasonic generators of the frequencies or ultrasonic waves and also it can be used in the crystal oscillator and the second parts we have discussed a very important, a pneumatic system which is called the flapper nozzle systems with feedback systems, right and it is very fail safe devices as you can, if you compare with electrical devices it never fails actually, this, except the routine maintenance of the orifice, because entire operation depends on the orifice width also. So, diameter of the orifice also is very important.

Over the long use it should not, it should not widen, so that you have to change, you have to make the change in entire calibration, otherwise it is a just fail set device. It never, it

never happens that it is not working or it fails. So, that is the great advantage of this type of pneumatic system. For this reason it is used over the years in the industry and still it is used in some of the industries like hydrocarbon industry, where high voltage is restricted. That means I cannot use a voltage or any devices which has a voltage more than 40 volt, because you know there is a, there is a large, you should have a large actuator or large valve control bulb.

I need a voltage of at least of 220 volt to create a large torque. That is not possible because that voltage is not allowed in the hydrocarbon industry. Though the transmitter side of the electrical that is fine, but the basic actuator, basic sensor there are the basic pneumatic, because it is totally hazardous free, right? Because so many supply we have instead of electrical supply, so we have a pneumatic supply there, right? So, with this I come to the end of the lesson 24.