Module 5

DC to AC Converters

Lesson 40

Load-commutated Current Source Inverter (CSI)

Instructional Objectives

Study of the circuit and operation for Load-commutated Current Source Inverter (CSI)

Introduction

In the last lesson (5.7) – seventh one in this module, the circuit and operation of single-phase and three-phase Current Source Inverters (CSI), with relevant waveforms, have been described in detail. The device used is thyristor. The type is the Auto-Sequential Commutated Inverter (ASCI). In this lesson (5.8) – eighth and final one in this module, the circuit and operation of load-commuted CSI, including waveforms, will be presented in detail.

Keywords: Load-commutated current source inverter (CSI)

Load-Commutated CSI

In the last lesson, ASCI mode of operation for a single-phase Current Source Inverter (CSI) was presented. Two commutating capacitors, along with four diodes, are used in the above circuit for commutation from one pair of thyristors to the second pair. Earlier, also in VSI, if the load is capacitive, it was shown that forced commutation may not be needed. The operation of a single-phase CSI with capacitive load (Fig. 40.1) is discussed here. It may be noted that the capacitor, C is assumed to be in parallel with resistive load (R). The capacitor, C is used for storing the charge, or voltage, to be used to force-commutate the conducting thyristor pair as will be shown. As was the case in the last lesson, a constant current source, or a voltage source with large inductance, is used as the input to the circuit.

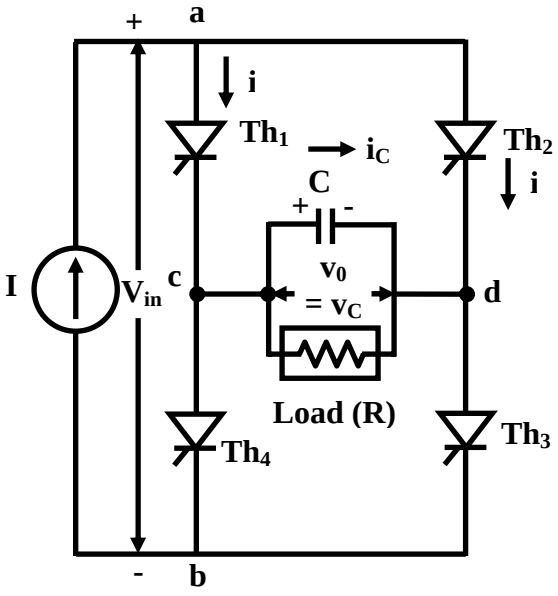

Fig. 40.1: Load-commuted CSI

The power switching devices used here is the same, i.e. four thyristors only in a full- bridge configuration. The positive direction for load current and voltage, is shown in Fig. 40.1. Before t = 0, the capacitor voltage is $v_C = -V_1$, i.e. the capacitor has left plate negative and right plate positive. At that time, the thyristor pair, Th_2 & Th_4 was conducting. When (at t = 0), the thyristor

pair, Th_1 & Th_3 is triggered by the pulses fed at the gates, the conducting thyristor pair, Th_2 & Th_4 is reverse biased by the capacitor voltage $v_C = -V_1$, and turns off immediately. The current path is through Th_1, load (parallel combination of R & C), Th_3, and the source. The current in the thyristors is $i_{Th1} = i_{Th3} = I$, the output current is $i_{ac} = I$; the capacitor voltage, v_C changes from $-V_1$ to V_1, as the capacitor gets charged by the current i_C during the time, $(T/2) > t > 0$. The load voltage is $v_0 = v_C$. Thus, the waveform of the current, $i_0 = (v_0 / R) = (v_C / R)$ through load resistance, R has the same nature as that of v_C (Fig. 40.2). Similarly, when (at $t = T/2$), the thyristor pair, Th_2 & Th_4 is triggered by the pulses fed at the gates, the conducting thyristor pair, Th_1 & Th_3 is reverse biased by the capacitor voltage $v_C = V_1$, and turns off immediately. The current path is through Th_2, load (parallel combination of R & C), Th_4, and the source. The current in the thyristors is $i_{Th2} = i_{Th4} = I$, but the output current is $i_{ac} = -I$; the capacitor voltage, v_C changes from V_1 to $-V_1$, as the capacitor gets charged by the current i_C during the time, $T > t > (T/2)$.

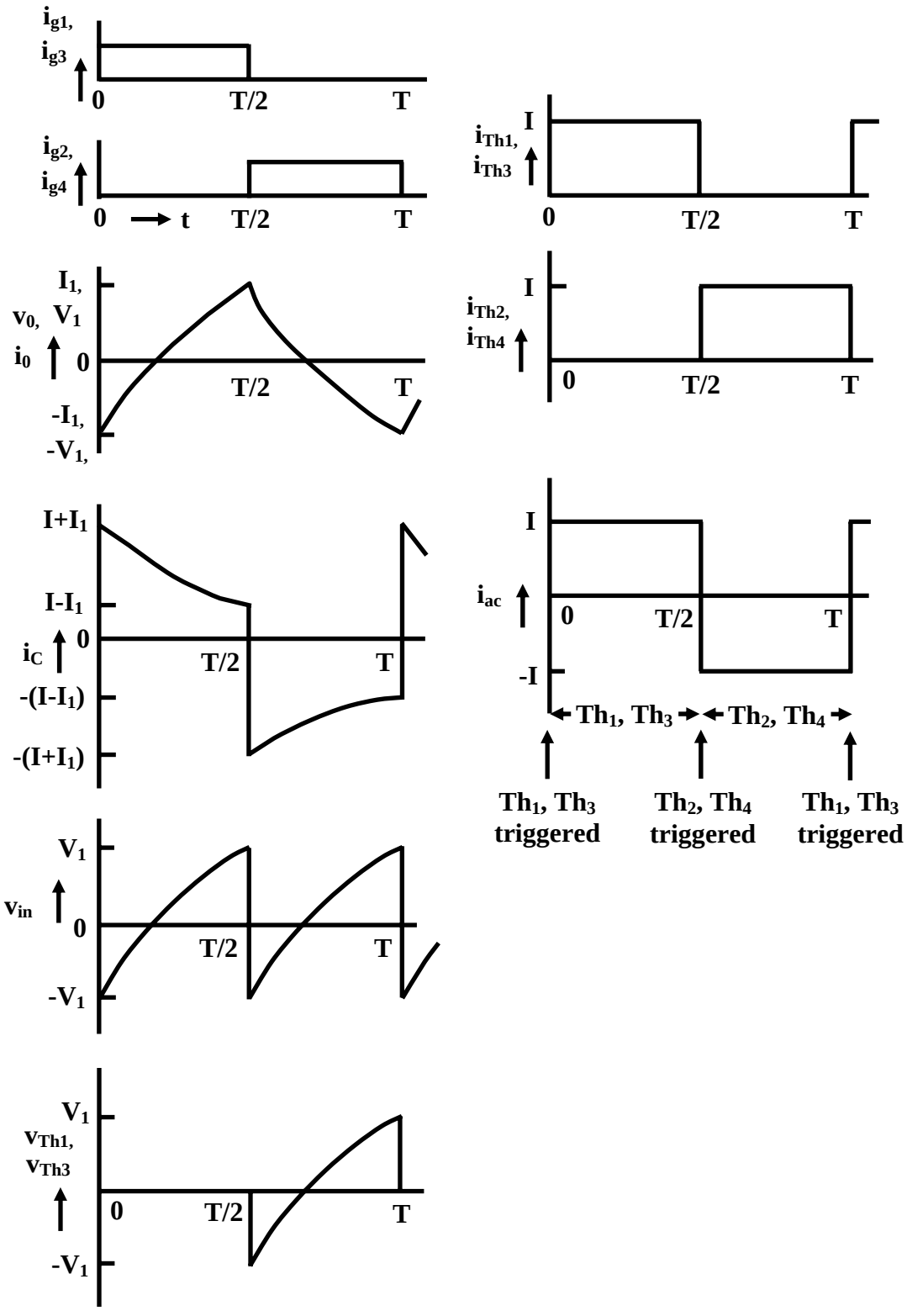

Fig. 40.2: Voltage and current waveforms.

Various current and voltage waveforms during one cycle $T > t > 0$, are shown in Fig. 40.2. At t = 0, the capacitor voltage is $v_C = -V_1$, then $v_0 = v_C = -V_1$, and the load current through R is $i_0 = -(V_1 / R) = -I_1$. As stated earlier, during the time $(T/2) > t > 0$, the capacitor gets charged, with its voltage changing from $-V_1$ to V_1. So, At $t = T/2$, the load current is $i_0 = (v_C / R) = (v_0 / R) = (V_1 / R) = I_1$. The input voltage is $v_{in} = v_0$, during $(T/2) > t > 0$, and $v_{in} = -v_0$, during $T > t > (T/2)$.

It may be observed that, when the thyristor pair, Th_1 & Th_3 is conducting for $(T/2) > t > 0$, the currents i_C, i_0 are leaving node A (Fig. 40.1), and the current, I is entering node A. Therefore, the equivalent circuit for $(T/2) > t > 0$, is shown in Fig. 40.3a. The current in node A, is $i_C + i_0 = I$ or, $i_C = I - i_0$. At t = 0, $i_0 = -I_1$, and $i_C = I + I_1$. The mathematical steps for a steady solution of the output current, and other parameters, such as input voltage etc., are given later. Just after (T/2), when the thyristor pair, Th_2 & Th_4 is conducting, the currents i_C, i_0 are entering node B (Fig. 40.1), and so also the current, I. The equivalent circuit for $T > t > (T/2)$, is shown in Fig. 40.3b. The current in node B is $i_C + i_0 + I = 0$ or, $i_C = -(I + i_0)$. At t = (T/2), $i_0 = I_1$, and $i_C = -(I + I_1)$. The cycle repeats itself.

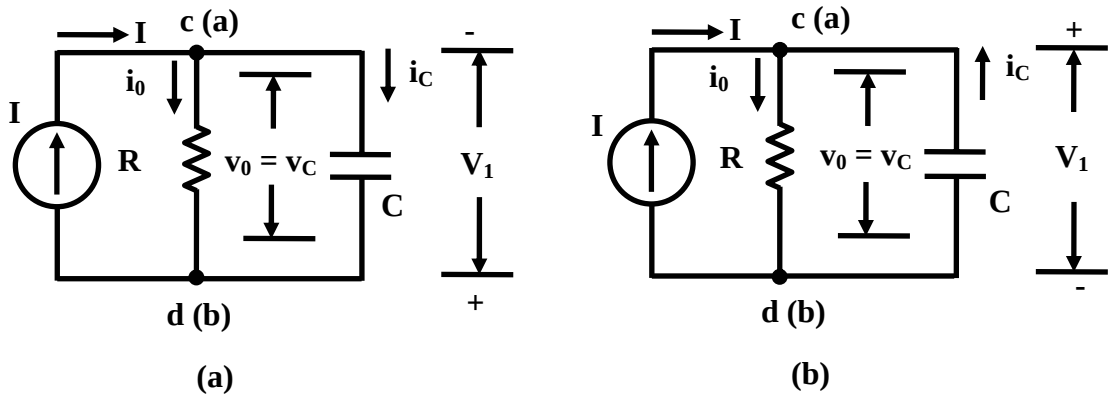

Fig. 40.3: (a) Equivalent circuit for 0 < t < T/2
(b) Equivalent circuit for T/2 < t < T

The steps to be followed to find the expression of the output current, and other parameters are described. The voltage balance equation for the equivalent circuit (Fig. 40.3a) is, $R \cdot i_0 - (1/C) \cdot \int (I - i_0)\, dt + v_1 = 0$

Differentiating it, we get $R \cdot \dfrac{d i_0}{dt} + \dfrac{i_0}{C} = \dfrac{I}{C}$

Solving it, with the initial condition for i_0 as given earlier,

$i_0 = I \cdot \left(1 - e^{-t/(R \cdot C)}\right) - I_1 \cdot e^{-t/(R \cdot C)}$

To arrive at a steady solution only, the following steps are followed. At t = (T/2), the current is $i_0 = I_1$, as shown later. So, $I_1 = I \cdot \left(1 - e^{-T/(2 \cdot R \cdot C)}\right) - I_1 \cdot e^{-T/(2 \cdot R \cdot C)}$

or, $I_1 = I \cdot \left[\dfrac{1 - e^{-T/(2 \cdot R \cdot C)}}{1 + e^{-T/(2 \cdot R \cdot C)}}\right] = I$, if $\left(T/(2 \cdot R \cdot C)\right) >> 1$ or, $T >> (R \cdot C)$

So, using the above expression, the output current, or the current in resistance, R comes out as,

$$i_0 = I \cdot \left[1 - \frac{2 \cdot \left(e^{-t/(R \cdot C)}\right)}{1 + e^{-T/(2 \cdot R \cdot C)}}\right]$$

The output voltage v_0, or the capacitor voltage v_C is,

$$v_0 = v_C = i_0 \cdot R = (R \cdot I) \cdot \left[1 - \frac{2 \cdot \left(e^{-t/(R \cdot C)}\right)}{1 + e^{-T/(2 \cdot R \cdot C)}}\right]$$

The turn-off time provided by the circuit for each thyristor is obtained from the condition that, when $t = t_{OFF}$, $v_0 = v_C = i_0 \cdot R = 0$. So,

$$v_0 = v_C = i_0 \cdot R = (R \cdot I) \cdot \left[1 - \frac{2 \cdot \left(e^{-t_{OFF}/(R \cdot C)}\right)}{1 + e^{-T/(2 \cdot R \cdot C)}}\right] = 0$$

or, $e^{-t_{OFF}/(R \cdot C)} = \left(1 + e^{-T/(2 \cdot R \cdot C)}\right)/2$

or, $t_{OFF} = (R \cdot C) \cdot \log_e\left(\frac{2}{1 + e^{-T/(2 \cdot R \cdot C)}}\right) = -(R \cdot C) \cdot \log_e\left[\left(1 + e^{-T/(2 \cdot R \cdot C)}\right)/2\right]$

The average value of the input voltage, V_{in} is,

$$V_{in} = \left(\frac{1}{T/2}\right) \cdot \int_0^{T/2} (i_0 \cdot R)\, dt = \left(\frac{2 \cdot I \cdot R}{T}\right) \cdot \int_0^{T/2} \left[1 - \frac{2 \cdot \left(e^{-t/(R \cdot C)}\right)}{1 + e^{-T/(2 \cdot R \cdot C)}}\right] dt$$

or, $V_{in} = (I \cdot R) \cdot \left[1 - \left(\frac{4 \cdot R \cdot C}{T}\right) \cdot \left(\frac{1 - e^{-T/(2 \cdot R \cdot C)}}{1 + e^{-T/(2 \cdot R \cdot C)}}\right)\right]$

When the input power ($V_{in} \cdot I$) is positive, power is delivered to the load.

The following points may be noted.

1. It may be observed from the equation given earlier that, as the inverter frequency ($f = 1/T$) is increased, the turn-off time provided by the circuit decreases. But, the circuit commutation time, t_{off}, should be more than the turn-off time of the thyristor, t_q, for reliable operation. This means that there is an upper limit to the inverter frequency, beyond which the thyristors in the inverter circuit will fail to commutate.

2. When the inverter frequency ($f = 1/T$) is low, or time period, T is high, the graph of $i_0(t)$ or $v_0(t)$ as given in Fig. 40.2, becomes flatter as shown by dotted line in Fig. 40.4. As this graph is nearer to a square wave, it can be inferred that, for low inverter frequencies, the inverter has square wave output for load current or load voltage (i_0 / v_0).

   When the inverter frequency ($f = 1/T$) is high, or time period, T is low, the waveform of v_0 or i_0 is shown by full line in Fig. 40.4. As this graph is closer to a sine wave, it can be noted that, for higher frequency, the CSI has sinusoidal wave shape for load (output) current or voltage.

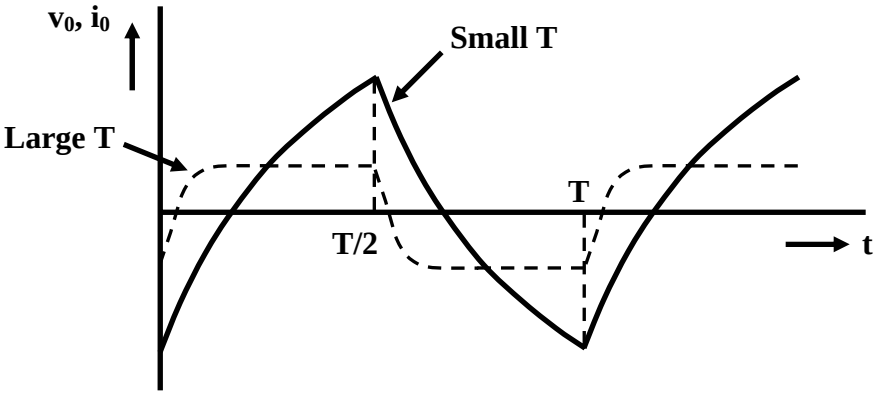

Fig. 40.4: Waveforms for CSI with resistive (R) load

(a) **Square wave output:** It has been found that, for obtaining square wave of the load current, $T/(2RC) > 5.0$. If t_q is the turn-off time for the thyristors used in CSI, then form the equation given earlier,

$t_q = (RC)\log_e\left(2/(1+e^{-5})\right) \approx (RC)\log_e 2 = 0.69(RC)$

or, $C = t_q/(0.69R)$

For $T/(2RC) = 5.0$ or $T = 10RC$, the maximum frequency is,

$f_{\max} = 1/T = 1/(10RC)$

Substituting the value of C obtained earlier, $f_{\max} = 0.069/t_q$

(b) **Sinusoidal wave output: F**or obtaining sinusoidal wave of the load current, the capacitive reactance, X_C at three times the minimum frequency, $f_{\min}$, should be lower than $R/2$, i.e.,

at $3f_{\min}$, $\quad X_C = \dfrac{1}{2\pi 3 f_{\min} C} \le \dfrac{R}{2}$,

or $C \ge 0.106/(R f_{\min})$

The inverter should therefore be operated at frequencies higher than $f_{\min}$ in order to obtain the sinusoidal wave shape.

In this lesson (5.8) – eighth and final one in this (last) module (5), the circuit and operation, of load-commuted CSI, including waveforms, are discussed in detail. In this module (5), mainly two types of dc-ac converters, termed as inverters – Voltage Source (VSI) and Current Source (CSI), have been presented. Both single-phase and three-phase inverters have been described, with relevant waveforms. Starting with the use of Pulse Width Modulation (PWM) techniques, used for voltage control in VSI, other variations, such as Sine PWM, have been taken up. Incidentally, this is the last lesson for the course on 'Power Electronics'.