Module 5

DC to AC Converters

Lesson 33

Introduction to Voltage Source Inverters

After completion of this lesson the reader will be able to:

(i) Identify the essential components of a voltage source inverter.
(ii) Explain the principle behind dc to ac conversion.
(iii) Identify the basic topology of single-phase and three-phase inverters and explain its principle of operation.
(iv) Explain the gate drive circuit requirements of inverter switches.

The word 'inverter' in the context of power-electronics denotes a class of power conversion (or power conditioning) circuits that operates from a dc voltage source or a dc current source and converts it into ac voltage or current. The 'inverter' does reverse of what ac-to-dc 'converter' does **(refer to ac to dc converters)**. Even though input to an inverter circuit is a dc source, it is not uncommon to have this dc derived from an ac source such as utility ac supply. Thus, for example, the primary source of input power may be utility ac voltage supply that is 'converted' to dc by an ac to dc converter and then 'inverted' back to ac using an inverter. Here, the final ac output may be of a different frequency and magnitude than the input ac of the utility supply.

[The nomenclature 'inverter' is sometimes also used for ac to dc converter circuits if the power flow direction is from dc to ac side. However in this lesson, irrespective of power flow direction, 'inverter' is referred as a circuit that operates from a stiff dc source and generates ac output. If the input dc is a voltage source, the inverter is called a voltage source inverter (VSI). One can similarly think of a current source inverter (CSI), where the input to the circuit is a current source. The VSI circuit has direct control over 'output (ac) voltage' whereas the CSI directly controls 'output (ac) current'. Shape of voltage waveforms output by an ideal VSI should be independent of load connected at the output.]

The simplest dc voltage source for a VSI may be a battery bank, which may consist of several cells in series-parallel combination. Solar photovoltaic cells can be another dc voltage source. An ac voltage supply, after rectification into dc will also qualify as a dc voltage source. A voltage source is called stiff, if the source voltage magnitude does not depend on load connected to it. All voltage source inverters assume stiff voltage supply at the input.

Some examples where voltage source inverters are used are: uninterruptible power supply (UPS) units, adjustable speed drives (ASD) for ac motors, electronic frequency changer circuits etc. Most of us are also familiar with commercially available inverter units used in homes and offices to power some essential ac loads in case the utility ac supply gets interrupted. In such inverter units, battery supply is used as the input dc voltage source and the inverter circuit converts the dc into ac voltage of desired frequency. The achievable magnitude of ac voltage is limited by the magnitude of input (dc bus) voltage. In ordinary household inverters the battery voltage may be just 12 volts and the inverter circuit may be capable of supplying ac voltage of around 10 volts (rms) only. In such cases the inverter output voltage is stepped up using a transformer to meet the load requirement of, say, 230 volts.

33.1 How to Get AC Output From DC Input Supply?

Figs. 33.1(a) and 33.1(b) show two schematic circuits, using transistor-switches, for generation of ac voltage from dc input supply. In both the circuits, the transistors work in common emitter configuration and are interconnected in push-pull manner. In order to have a single control signal

for the transistor switches, one transistor is of n-p-n type and the other of p-n-p type and their emitters and bases are shorted as shown in the figures. Both circuits require a symmetrical bipolar dc supply. Collector of n-p-n transistor is connected to positive dc supply (+E) and that of p-n-p transistor is connected to negative dc supply of same magnitude (-E). Load, which has been assumed resistive, is connected between the emitter shorting point and the power supply ground.

In Fig. 33.1(a), the transistors work in active (amplifier) mode and a sinusoidal control voltage of desired frequency is applied between the base and emitter points. When applied base signal is positive, the p-n-p transistor is reverse biased and the n-p-n transistor conducts the load current. Similarly for negative base voltage the p-n-p transistor conducts while n-p-n transistor remains reverse biased. A suitable resistor in series with the base signal will limit the base current and keep it sinusoidal provided the applied (sinusoidal) base signal magnitude is much higher than the base to emitter conduction-voltage drop. Under the assumption of constant gain (h_{fe}) of the transistor over its working range, the load current can be seen to follow the applied base signal. Fig. 33.2(a) shows a typical load voltage (in blue color) and base signal (green color) waveforms. This particular figure also shows the switch power loss for n-p-n transistor (in brown color). The other transistor will also be dissipating identical power during its conduction. The quantities in Fig. 33.2(a) are in per unit magnitudes where the base values are input supply voltage (E) and the load resistance (R). Accordingly the base magnitudes of current and power are E/R and E^2/R respectively. As can be seen, the power loss in switches is a considerable portion of circuit's input power and hence such circuits are unacceptable for large output power applications.

As against the amplifier circuit of Fig. 33.1(a), the circuit of Fig. 33.1(b) works in switched mode. The conducting switch remains fully on having negligible on-state voltage drop and the non-conducting switch remains fully off allowing no leakage current through it. The load voltage waveform output by switched-mode circuit of Fig. 33.1(b) is rectangular with magnitude +E when the n-p-n transistor is on and –E when p-n-p transistor is on. Fig. 33.2(b) shows one such waveform (in pink color). The on and off durations of the two transistors are controlled so that (i) the resulting rectangular waveform has no dc component (ii) has a fundamental (sinusoidal) component of desired frequency and magnitude and (iii) the frequencies of unwanted harmonic voltages are much higher than that of the fundamental component. The fundamental sine wave in Fig. 33.2(b), shown in blue color, is identical to the sinusoidal output voltage of Fig. 33.2(a).

Both amplifier mode and switched mode circuits of Figs. 33.1(a) and 33.1(b) are capable of producing ac voltages of controllable magnitude and frequency, however, the amplifier circuit is not acceptable in power-electronic applications due to high switch power loss. On the other hand, the switched mode circuit generates significant amount of unwanted harmonic voltages along with the desired fundamental frequency voltage. As will be shown in some later lessons, the frequency spectrum of these unwanted harmonics can be shifted towards high frequency by adopting proper switching pattern. These high frequency voltage harmonics can easily be blocked using small size filter and the resulting quality of load voltage can be made acceptable.

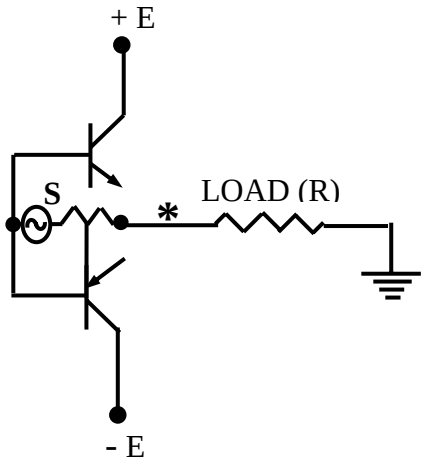

Fig. 33.1 (a): A push-pull active amplifier circuit

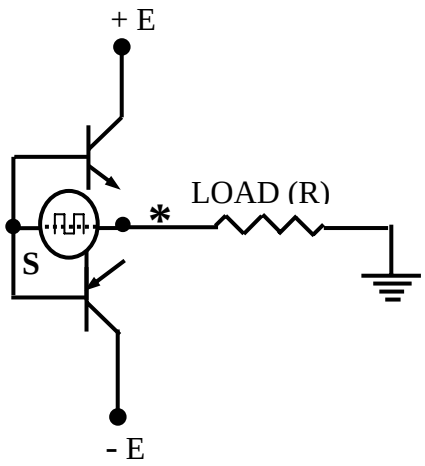

Fig. 33.1 (b): A push-pull switched mode circuit

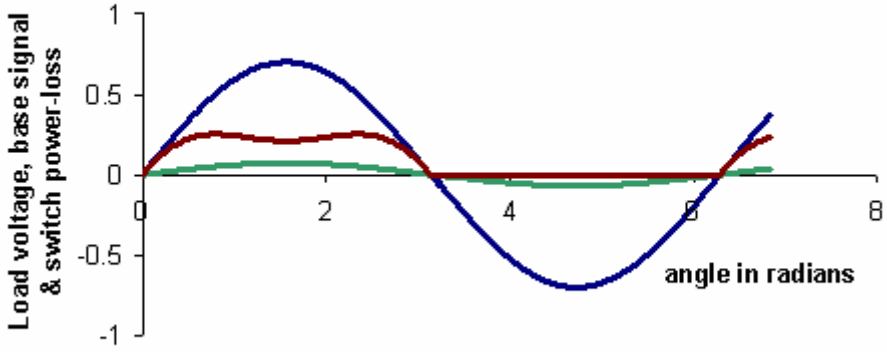

Fig. 33.2(a): Switch in amplifier mode operation

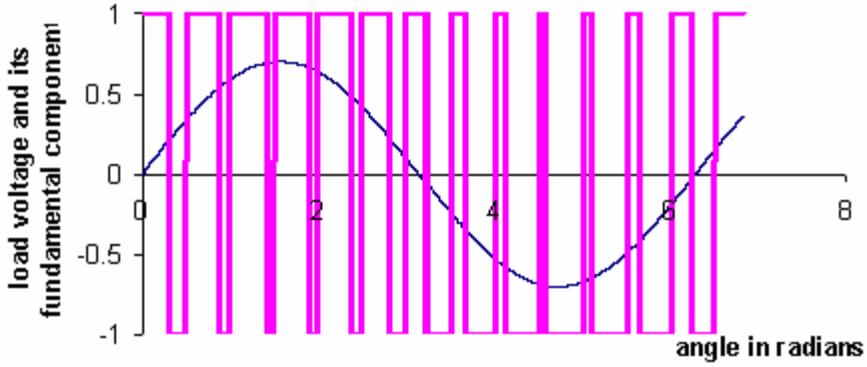

Fig. 33.2(b): Switched mode (inverter) operation

The magnitude, phase and frequency of the fundamental voltage waveform in Fig. 33.2(b) is solely determined by the magnitude of supply voltage and the switching pattern of the push-pull circuit shown in Fig. 33.1(b). Thus, as long as the transistors work in the switch-mode (fully on or fully off), the output voltage is essentially load-independent.

33.2 What If The Load Is Not Resistive?

Circuit of Fig. 33.1(b) will not be able to output proper voltage waveform for a non-resistive load for the reasons mentioned below.

Transistors used in the circuit of Fig. 33.1(b) are meant to carry only unidirectional current (from collector to emitter) and thus if the upper (n-p-n) transistor is on, the current must enter the star (*) marked terminal of the load and this same terminal will get connected to the positive dc supply (+E), other load terminal being at ground potential. When n-p-n transistor turns off and p-n-p type turns on, the load voltage and current polarities reverse simultaneously (p-n-p transistor can only carry current coming out of star marked end of load). Such one to one matching between the instantaneous polarities of load voltage and load current can be achieved only in purely resistive loads. For a general load the instantaneous current polarity may be different from instantaneous load-voltage polarity. As pointed out in section 33.1, the inverter switching-pattern fixes the output waveform irrespective of the load. Thus the magnitude, phase and frequency of the fundamental voltage output by a VSI is independent of the nature of load. Thus it turns out that for a non-resistive load the switches in the circuit of Fig. 33.1(b) should be able to carry bi-directional current and at the same time be controllable. **[A mechanical switch realized using an electromagnetic contactor is one example of the bi-directional current carrying controllable switch. However electromagnetic contactors are not capable of operating at high frequency, in the range of kilohertz, and may not be suitable for present application.]** If an anti-parallel diode is connected across each transistor switch, as shown in Fig. 33.3(a), the combination can conduct a bi-directional current. Now the transistor in anti-parallel with the diode may be considered as a single switch. **[A major difference exists between this bi-directional electronic switch and a bi-directional current carrying mechanical switch. The mechanical switch can be subjected to bi-directional voltage. When off, the mechanical switch can block both positive and negative voltage across its terminals. The electronic switch of Fig. 33.3(a) can block only one polarity of voltage, the one that keeps the diode reverse biased. Under this polarity of voltage the switch can remain off as long as the base (or the gate) terminal is not given the turn-on signal. When applied voltage polarity is reversed the diode starts conducting and so the switch is not able to block the flow of reverse current.]** In spite of unidirectional voltage blocking capability, the new electronic switch (similar to the one shown in Fig. 33.3(a)) suffices for the inverter application as pointed out in the following paragraphs.

The push-pull circuit operation is now revisited using bi-directional current carrying switches. The modified circuit is shown in Fig. 33.3(b). It may be noted that both IGBT and BJT type transistors, when bypassed by anti-parallel diode, qualify as bi-directional current carrying switches. However, IGBT switch is controlled by gate voltage whereas the BJT

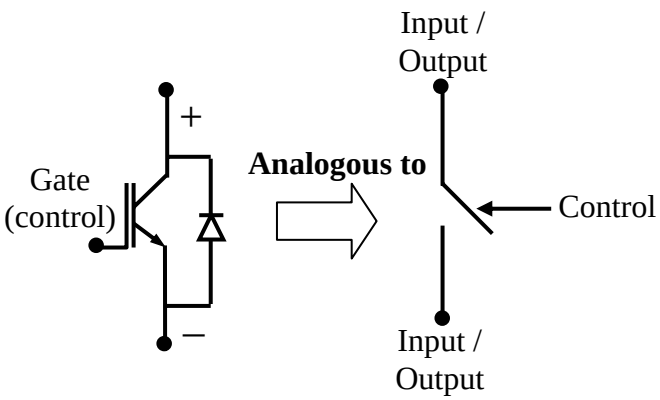

Fig. 33.3(a): Bi-directional controlled switch

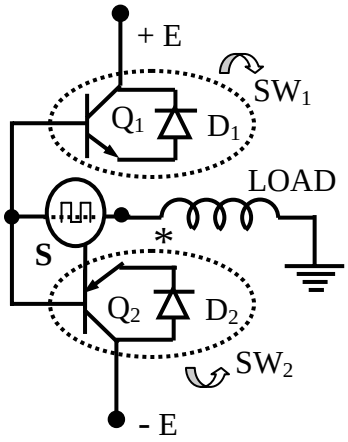

Fig. 33.3 (b): Modified push-pull circuit

switch is controlled using base current. **[IGBT switches are easier to use, are much faster and are available in higher voltage and current ratings. As a result BJT switches are becoming obsolete.]** In the circuit of Fig. 33.3(b), n-p-n transistor (Q_1) together with diode (D_1) constitutes the upper switch (SW_1). Similarly lower switch (SW_2) consists of p-n-p transistor (Q_2) in anti-parallel with diode (D_2). By applying positive base-to-emitter voltage of suitable magnitude to transistor 'Q_1', the upper switch is turned on. Once the upper switch (diode 'D_1'or transistor 'Q_1') is conducting star end of load is at '+E' potential and diode 'D_2' of lower switch gets reverse biased. Transistor 'Q_2' is also reverse biased due to application of positive base voltage to the transistors. Thus while switch 'SW_1'is conducting current, switch 'SW_2' is off and is blocking voltage of magnitude '2E'. Similarly when applied base voltage to the transistors is made negative, 'Q_1' is reverse biased and 'Q_2' is forward biased. This results in 'SW_1' turning off and 'SW_2' turning on. Now 'SW_1' blocks a voltage of magnitude '2E'.

It may be interesting to see how diodes follow the switching command given to the transistor part of the switches. To illustrate this point some details of circuit operation with an inductive load, consisting of a resistor and an inductor in series, is considered. As is well known, current through such loads cannot change abruptly. The electrical inertial time constant of the load, given by its L (inductance) / R (resistance) ratio, may in general be large compared to the chosen switching time period of the transistor switches. Thus the transistors 'Q_1' and 'Q_2' may turn-on and turn-off several times before the load current direction changes. Let us consider the time instant when instantaneous load current is entering the star end of the load in Fig. 33.3(b). Now with the assumed load current direction when 'Q_1' is given turn-on signal current flows from positive dc supply, through transistor 'Q_1', to load. Next, when 'Q_1' is turned-off and 'Q_2' is turned on (but load current direction remaining unchanged) the load current finds its path through diode of lower switch (D_2). Whether 'D_2' or 'Q_2' conducts, voltage drop across 'SW_2' is virtually zero and it can be considered as a closed or a fully-on switch. In the following switching cycle when 'Q_1' is turned on again (load current direction still unchanged) the load current path reverts back from 'D_2' to 'Q_1'. It may not be difficult to see how this happens. While current flowed through 'D_2' the load circuit got connected to negative emf (-E) of the supply. When 'Q_1' conducts the positive (+E) emf supports the load current. The natural choice for load current is to move from 'D_2' to 'Q_1'. In fact turning on of 'Q_1' will make 'D_2' reverse biased. The reader may repeat a similar exercise when the instantaneous load current comes out of the star end of load. Thus it will be evident that diodes do not need a separate command to turn on and off. Irrespective of the load current direction, turning on of 'Q_1' makes 'SW_1' on and

similarly turning off of 'Q_1' (with simultaneous turn-on of 'Q_2') makes 'SW_2'on. 'Q_1' and 'Q_2' are turned on in a complementary manner. It may not be difficult to see that the circuit of Fig. 33.3(b) will work satisfactorily for a purely resistive load and a series connected resistor-capacitor load too.

The push-pull circuit of Fig. 33.3(b) has some technical demerits that have been discussed below.

First, it needs a bipolar dc supply with identical magnitudes of positive and negative supply voltages. For practical reasons it would have been simpler if only one (uni-polar) dc source was required. In fact some circuit topologies realize a bi-polar dc supply by splitting the single dc voltage-source through capacitive potential divider arrangement. **[A resistive potential divider will be terribly inefficient.]** Two identical capacitors of large magnitude are put across the dc supply and the junction point of the capacitors is used as the neutral (ground) point of the bi-polar dc supply. Fig. 33.3(c) shows one such circuit where a single dc supply has been split in two halves. In such circuits the voltages across the two capacitors may not remain exactly balanced due to mismatch in the loading patterns or mismatch in leakage currents of the individual capacitors. Also, unless the capacitors are of very large magnitude, there may be significant ripple in the capacitor voltages, especially at low switching frequencies. The requirement of splitting a single dc source is eliminated if a full bridge circuit, as mentioned in the next section, is used.

The second demerit of the push-pull circuit shown in Fig. 33.3(b) is the requirement of two different kinds of transistors, one n-p-n type and the other p-n-p type. The switching speeds of n-p-n and p-n-p transistors are widely different unless they are produced carefully as matched pairs. In power electronic applications, n-p-n transistors are preferred as they can operate at higher switching frequencies. Similarly n-channel MOSFETs and IGBTs are preferred over their p-channel counterparts. The difficulty in using two n-p-n transistors in the above discussed push-pull circuit is that they can no longer have a common base and a common emitter point and thus it won't be possible to have a single base drive signal for controlling both of them. The base signals for the individual transistors will then need to be separate and isolated from each other. The difficulty in providing isolated base signals for the two transistors is, often, more than compensated by the improved capability of the circuit that uses both n-p-n transistors or n-channel IGBTs. The circuit in Fig. 33.3(c) shows identical transistors (n-channel IGBTs) for both upper and lower switches. The gate drive signals of the two transistors (IGBTs) now need to be different and isolated as the two emitter points are at different potentials. The circuit in Fig. 33.3(c) is better known as a half bridge inverter.

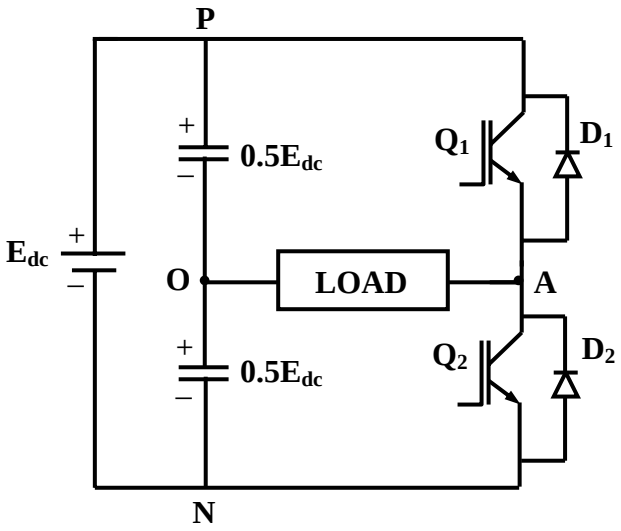

Fig. 33.3(c): Topology of a 1-phase half bridge VSI

33.3 General Structure of Voltage Source Inverters

Figs. 33.4 (a) and 33.4(b) show the typical power-circuit topologies of a single-phase and a three-phase voltage source inverter respectively. These topologies require only a single dc source and for medium output power applications the preferred devices are n-channel IGBTs. 'E_{dc}' is the input dc supply and a large dc link capacitor (C_{dc}) is put across the supply terminals. Capacitors and switches are connected to dc bus using short leads to minimize the stray inductance between the capacitor and the inverter switches. Needless to say that physical layout of positive and negative bus lines is also important to limit stray inductances. Q_1, Q_2, Q_3 etc. are fast and controllable switches. D_1, D_2, D_3 etc. are fast recovery diodes connected in anti-parallel with the switches. 'A', 'B' and 'C' are output terminals of the inverter that get connected to the ac load. A three-phase inverter has three load-phase terminals whereas a single-phase inverter has only one pair of load terminals.

The current supplied by the dc bus to the inverter switches is referred as dc link current and has been shown as 'i_{dc}' in Figs 33.4(a) and 33.4(b). The magnitude of dc link current often changes in step (and some times its direction also changes) as the inverter switches are turned on and off. The step change in instantaneous dc link current occurs even if the ac load at the inverter output is drawing steady power. However, average magnitude of the dc link current remains positive if net power-flow is from dc bus to ac load. The net power-flow direction reverses if the ac load connected to the inverter is regenerating. Under regeneration, the mean magnitude of dc link current is negative. **[The dc link current may conceptually be decomposed into its dc and ac components. The individual roles of the 'dc voltage source' and the 'dc link capacitor' may be clearly seen with respect to the dc and ac components of the dc link current. For the dc component of current the capacitor acts like open circuit. As expected, under steady state, the capacitor does not supply any dc current. The dc part of bus current is supplied solely by the dc source. A practical dc voltage source may have some resistance as well as some inductance in series with its internal emf. For dc component of bus current, the source voltage appears in series with its internal resistance (effect of source inductance is not felt). But for ac component of current, the internal dc emf of source appears as short and its series impedance (resistance in series with inductance) appears in parallel with the dc-link**

capacitor. Thus the ac component of current gets divided into these two parallel paths. However, the high frequency component of ac current mainly flows through the capacitor, as the capacitive impedance is lower at high frequencies. The step change in dc link current is associated with significant amount of high frequency components of current that essentially finds its path through the capacitor.]

For an ideal input (dc) supply, with no series impedance, the dc link capacitor does not have any role. However a practical voltage supply may have considerable amount of output impedance. The supply line impedance, if not bypassed by a sufficiently large dc link capacitor, may cause considerable voltage spike at the dc bus during inverter operation. This may result in deterioration of output voltage quality, it may also cause malfunction of the inverter switches as the bus voltage appears across the non-conducting switches of the inverter. Also, in the absence of dc link capacitor, the series inductance of the supply line will prevent quick build up or fall of current through it and the circuit behaves differently from the ideal VSI where the dc voltage supply is supposed to allow rise and fall in current as per the demand of the inverter circuit.

[It may not be possible to reduce supply line inductance below certain limit. Most dc supplies will inherently have rather significant series inductance, for example a conventional dc generator will have considerable armature inductance in series with the armature emf. Similarly, if the dc supply is derived after rectifying ac voltage, the ac supply line inductance will prevent quick change in rectifier output current. The effect of ac line inductance is reflected on the dc side as well, unless this inductance is effectively bypassed by the dc side capacitor. Even the connecting leads from the dc source to the inverter dc bus may contribute significantly to the supply line inductance in case the lead lengths are large and circuit lay out is poor. It may be mentioned here that an inductance, in series with the dc supply, may at times be welcome. The reason being that for some types of dc sources, like batteries, it is detrimental to carry high frequency ripple current. For such cases it is advantageous if the dc source has some series inductance. Due to series inductance of the source, the high frequency ripple will prefer to flow through the dc link capacitor and thus relieve the dc source.]

The dc link capacitor should be put very close to the switches so that it provides a low impedance path to the high frequency component of the switch currents. The capacitor itself must be of good quality with very low equivalent series resistor (ESR) and equivalent series inductor (ESL). The length of leads that interconnect switches and diodes to the dc bus must also be minimum to avoid insertion of significant amount of stray inductances in the circuit. The overall layout of the power circuit has a significant effect over the performance of the inverter circuit.

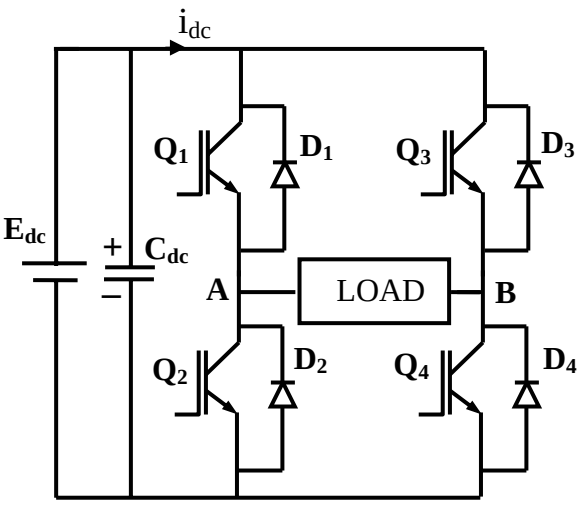

Fig. 33.4(a): Topology of a 1-phase VSI

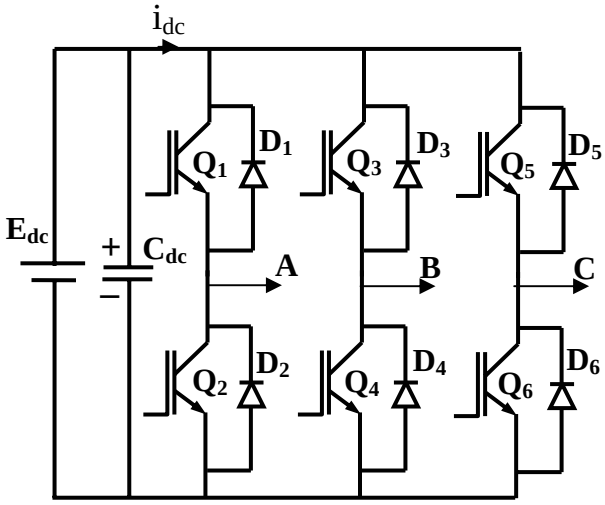

Fig. 33.4(b): Topology of a 3-phase VSI

[One of the thumb rules for good circuit layout is to put the conductor pairs carrying same magnitude but opposite direction of currents close by, the minimum distance between them being decided only by their voltage isolation requirement. Thus the positive and negative terminals of the dc bus should run close by. A twisted wire pair may be an example of two closely running wires.]

The details of the inverter circuits shown in Figs. 33.4(a) and 33.4(b) are discussed in later lessons. However it may be mentioned here that these circuits are essentially extension of the half bridge circuit shown in Fig. 33.3(c). For example, the single-phase bridge circuit of Fig. 33.4(a) may be thought of as two half-bridge circuits sharing the same dc bus. Thus the single phase 'full-bridge' (often, simply called as 'bridge') circuit has two legs of switches, each leg consisting of an upper switch and a lower switch. Junction point of the upper and lower switches is the output point of that particular leg. Voltage between output point of legs and the mid-potential of the dc bus is called as **'pole voltage'** referred to the mid potential of the dc bus. One may think of pole voltage referred to negative bus or referred to positive bus too but unless otherwise mentioned pole voltages are assumed to be referred to the mid-potential of the dc bus. The two pole voltages of the single-phase bridge inverter generally have same magnitude and frequency but their phases are 180^0 apart. Thus the load connected between these two pole outputs (between points 'A' and 'B') will have a voltage equal to twice the magnitude of the individual pole voltage. The pole voltages of the 3-phase inverter bridge, shown in Fig. 33.4(b), are phase apart by 120^0 each.

33.4 Need For Isolated Gate-Control Signals For The Switches

As already mentioned the switches in bridge configurations of inverters, as in Figs. 33.3(c), 33.4(a) and 33.4(b), need to be provided with isolated gate (or base) drive signals. The individual control signal for the switches needs to be provided across the gate (base) and source (or emitter) terminals of the particular switch. The gate control signals are low voltage signals referred to the source (emitter) terminal of the switch. For n-channel IGBT and MOSFET switches, when gate to source voltage is more than threshold voltage for turn-on, the switch turns on and when it is less than threshold voltage the switch turns off. The threshold voltage is generally of the order of +5 volts but for quicker switching the turn-on gate voltage magnitude is kept around +15 volts

where as turn-off gate voltage is zero or little negative (around –5 volts). It is to be remembered that the two switches of an inverter-leg are controlled in a complementary manner. When the upper switch of any leg is ‘on’, the corresponding lower switch remains ‘off’ and vice-versa. When a switch is ‘on’ its emitter and collector terminals are virtually shorted. Thus with upper switch ‘on’, the emitter of the upper switch is at positive dc bus potential. Similarly with lower switch ‘on’, the emitter of upper switch of that leg is virtually at the negative dc bus potential. Emitters of all the lower switches are solidly connected to the negative line of the dc bus. Since gate control signals are applied with respect to the emitter terminals of the switches, the gate voltages of all the upper switches must be floating with respect to the dc bus line potentials. This calls for isolation between the gate control signals of upper switches and between upper and lower switches. Only the emitters of lower switches of all the legs are at the same potential (since all of them are solidly connected to the negative dc bus) and hence the gate control signals of lower switches need not be isolated among themselves. As should be clear from the above discussion, the isolation provided between upper and lower switches must withstand a peak voltage stress equal to dc bus voltage. Gate-signal isolation for inverter switches is generally achieved by means of optical-isolator (opto-isolator) circuits. Fig.33.5 shows a typical opto-isolator circuit. The circuit makes use of a commercially available opto-coupler IC, shown within dotted lines in the figure. Input stage of the IC is a light emitting diode (LED) that emits light when forward biased. The light output of the LED falls on reverse biased junction of an optical diode. The LED and the photo-diode are suitably positioned inside the opto-coupler chip to ensure that the light emitted by the LED falls on the photo-diode junction. The gate control pulses for the switch are applied to the input LED through a current limiting resistor of appropriate magnitude. These gate pulses, generated by the gate logic circuit, are essentially in the digital form. A high level of the gate signal may be taken as ‘on’ command and a low level (at ground level) may be taken as ‘off’ command. Under this assumption, the cathode of the LED is connected to the ground point of the gate-logic card and anode is fed with the logic card output. The circuit on the output (photo-diode) side is connected to a floating dc power supply, as shown in Fig. 33.5. The control (logic card) supply ground is isolated from the floating-supply ground of the output. In the figure the two grounds have been shown by two different symbols. The schematic connection shown in the figure indicates that the photo-diode is reverse biased. A resistor in series with the diode indicates the magnitude of the reverse leakage current of the diode. When input signal to LED is high, LED conducts and the emitted light falls on the reverse biased p-n junction. Irradiation of light causes generation of significant number of electron-hole pairs in the depletion region of the reverse biased diode. As a result magnitude of reverse leakage current of the diode increases appreciably. The resistor connected in series with the photo-diode now has higher voltage drop due to the increased leakage current. A signal comparator circuit senses this condition and outputs a high level signal, which is amplified before being output. Thus an isolated and amplified gate signal is obtained and may directly be connected to the gate terminal of the switch (often a small series resistor, as suggested by the switch manufacturer, is put between the output signal and the gate terminal of the switch).

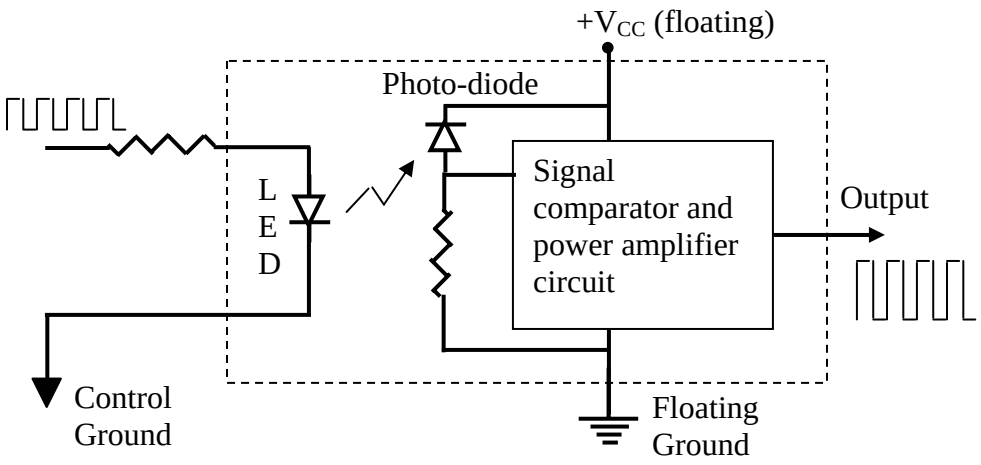

Fig.33.5: A schematic opto-isolator circuit

33.5 Classification of Voltage Source Inverters

Voltage source inverters can be classified according to different criterions. They can be classified according to number of phases they output. Accordingly there are single-phase or three-phase inverters depending on whether they output single or three-phase voltages. It is also possible to have inverters with two or five or any other number of output phases. Inverters can also be classified according to their ability in controlling the magnitude of output parameters like, frequency, voltage, harmonic content etc. Some inverters can output only fixed magnitude (though variable frequency) voltages whereas some others are capable of both variable voltage, variable frequency (VVVF) output. Output of some voltage source inverters is corrupted by significant amount of many low order harmonics like 3^{rd}, 5^{th}, 7^{th}, 11^{th}, 13^{th} order of the desired (fundamental) frequency voltage. Some other inverters may be free from low order harmonics but may still be corrupted by some high order harmonics. Inverters used for ac motor drive applications are expected to have less of low order harmonics in the output voltage waveform, even if it is at the cost of increased high order harmonics. Higher order harmonic voltage distortions are, in most ac motor loads, filtered away by the inductive nature of the load itself.

Inverters may also be classified according to their topologies. Some inverter topologies are suitable for low and medium voltage ratings whereas some others are more suitable for higher voltage applications. The inverters shown in Figs. 33.3(c), 33.4(a) and 33.4(b) are two level inverters as the pole voltages may acquire either positive dc bus or negative dc bus potential. For higher voltage applications it may not be uncommon to have three level or five level inverters.

Quiz Problems

1. A large capacitor, put across dc bus of a voltage source inverter, is intended to:
   (a) allow a low impedance path to the high frequency component of dc link current.
   (b) to minimize high frequency current ripple through the ideal dc source.
   (c) to maintain a constant dc link current.
   (d) to protect against switch failure.
2. A diode in anti-parallel with the controlled switch, like IGBT, is used in VSI to:
   (a) prevent reversal of dc link current.

(b) allow a non-unity power factor load at the output.
(c) protect the circuit against accidental reversal of dc bus polarity.
(d) none of the above.

3. The inverter switches work in fully-on or fully-off mode to achieve:
   (a) easier gate control circuit for the switching devices.
   (b) minimum distortion in the output voltage waveform.
   (c) reduced losses in the switches.
   (d) satisfactory operation for non-resistive load at the output.
4. Gate (base) signals to the VSI switches, using n-channel IGBTs, need to be isolated to allow:
   (a) protection of switches against short at the inverter output terminals.
   (b) switches to be connected in bridge fashion.
   (c) lower losses in the gate drive circuit.
   (d) a dc link voltage higher than the switch voltage rating.

(Answers to the quiz problems: 1-a, 2-b, 3-c, 4-b)