MOS Transistor - A Circuit View of a Device

Case I: \( V_G = V_S = V_D = V_B = 0 \ \text{Volt} \),

We observe \( I_{DS} = 0 \). Which means

Transistor is 'OFF'

In current technology node (say less than 90 nm) too, This is valid as Ohms Law cannot be violated
Case 2. \( V_{ds} = 0 \)

\( V_{s} = 0 \)
\( V_{ds} \) is Positive
\( V_{s} = 0 \)
\( V_{ds} = V_{bs} = 0 \)

But \( V_{ds} \) \( \Rightarrow \) Positive (\( \geq 0 \))

\( I_{ds} = 0 \) in Ideal Condition

as Both the Diodes Source/Bulk & Drain/Bulk are Reverse Biased

However in newer technologies due to reduced dimensions and increased doping in channel area, one observes \( I_{ds} \) is not negligible. Transistor is Partially 'ON' (Problem Case)
Case 3

\[ V_{gs} \text{ is Finite} \]
\[ V_{ds} = 0, \ V_{bs} = 0 \]

This is equivalent case of MOS capacitor

(i) \( V_{gs} < 0 \) \((-vc)\) \underline{Accumulation Mode} \[Q_{m} \]

Gate gets \(-vc\) charge \(-Q_{m}\)

Due to Gauss's Law
Semiconductor Surface below the dielectric layer, must produce equivalent + charge \(Q_{s}\), such that \(Q_{m} + Q_{s} = 0\)

As \(Q_{m} = -vc\)

Assumption \(Q_{ox} = 0\) \[Q_{s} \text{ is Positive} \]

Holes accumulate near interface
(iii) \( V_{GS} \) Positive & Small.

Hence 'Gate' Plane gets a charge \( +Q_m \).

By Gauss's Law

Now \( Q_s \) is \(-Ve\)

In P-Semiconductor \(-Ve\) \( Q_s \) can be obtained by holes getting depleted at the interface leaving \(-Ve\) charged Depletion layer due to ionised Acceptors \((-Q_{Na})\). This mode is called Depletion Mode.
Additional -ve charge is provided by free electrons at the interface. This layer of free electrons (-ve charge) is opposite that of substrate, giving +ive charges due to Holes. Hence this layer is called inversion layer (n-layer).

\[ V_{GS} = V_T = 2\phi_F - \frac{Q_s}{C_{ox}} = 2\phi_F + \frac{\epsilon N_A X_{dmax}}{C_{ox}} \]

Both terms on RHS are now Positive
i.e. \( V_T \) for \( n \)-channel device is Positive

Two Assumptions were made here
(i) \( Q_{ox} = 0 \)
(ii) \( \phi_{ms} = \phi_m - \phi_s = 0 \)

If we take these into account
\[ V_T = \phi_{ms} + 2\phi_F - \frac{Q_{ox}}{C_{ox}} - \frac{Q_s}{C_{ox}} \]
\[ V_s + V_{ox} = V_a s \]

\[ D = \varepsilon_s \varepsilon_s \]

\[ \varepsilon_s \varepsilon_s = \frac{E_{ox} E_{ox}}{t_{ox}} \]

\[ Q_s = -\varepsilon_s \varepsilon_s \]

\[ Q_m + Q_s + Q_{ox} = 0 \]

\[ Q_m = -Q_s - Q_{ox} \]

\[ V_{ox} = \frac{Q_s}{C_{ox}} \]

\[ V_T = 2\Phi - \frac{Q_s}{C_{ox}} \mid_{V_a = V_T} = 2\Phi - \frac{-2N_a^2 e t_{ox}}{C_{ox}} \]
\[
V_a \quad \frac{q}{S_{\text{ne}}}
\]

\[
\frac{d\varepsilon}{dx} = \frac{\varepsilon}{\varepsilon}
\]

\[
V_g = V_{0x} + \sqrt{\frac{q}{S_{\text{ne}}}}
\]

\[
\varepsilon = -\frac{dV}{dx}
\]

\[
\frac{qV_S}{kT}
\]

\[
\alpha \propto \varepsilon
\]
(iii) \( V_{GS} + \text{tire and substantial} \)

\[ V_{GS} + \text{tire} \]

\[ V_{DS} = 0 \]

\[ E_{ox} \]

\[ \text{Inversion} \]

\[ p (\text{Na conc}) \]

\[ V_{GS} \text{ + tire makes } Q_m \text{ substantially larger + tire} \]

However at a Value of \( V_{GS} = V_T \), the Depletion layer thickness \( x_d = \sqrt{\frac{2k_e E_0}{q^2 Na}} \) becomes maximum at \( \Phi_b = 2\Phi_f = 2kT \ln \frac{Na}{n_i} \) (2x Fermi Potential)

and Depletion Charge \( Q_B = -qNa x_d \text{max constant} \)

If \( V_{GS} \geq V_T \) then what is the Source \( Q \)-ve charge?
Intrinsic MOS Capacitor Model in Transistor

\[ \begin{align*}
C_{gs} & : 0 \quad \frac{1}{2}WL \cdot COX \\
C_{gd} & : 0 \quad \frac{1}{2}WL \cdot COX \\
C_{gb} & : \left( \frac{1}{3} \cdot \frac{VL \cdot L}{\sqrt{A}} + \frac{1}{WL} \right) \quad 0 \quad 0
\end{align*} \]

\[ C_{in} = C_{gs} + C_{gb} + C_{gd} \leq COX \text{ for all regions} \]
Assumption 2: 

\[ V = \mu (E(x)) \text{ is always true.} \]

In reality, \( V \rightarrow V_{\text{sat}} \)

Assumption 3: 

The \( I_{\text{DS}} \) current is wholly due to channel charge.

\( \rightarrow \) Only drift current occurs.

Though in very short channel devices in new structures diffusion currents may be contributing?!

Assumption 4: Even in Assumption 2, we have \( \mu \) constant?
Case 4:

\[ V_{GS} > V_T \quad V_{SB} = 0 \quad V_{DS} > 0 \quad V_S = 0 \]

Assumption 1: — Gradual Channel Approximation

\[ \varepsilon(x) \gg \varepsilon(y) \]

Channel charge is decided only by \( V_{GS} \)

or to say Inversion charge \( Q_n(y) = \varepsilon_n(x)(V_{GS} - V_T - V_S) \)

And \( I_{DS} = Q_n U \cdot W \quad ; \quad V = \mu \varepsilon(y) \)
With these First Order Assumptions

\[ I_{DS} = C_{ox} \left[ V_{GS} - V_T - V(y) \right] \mu \varepsilon W \]

\[ \varepsilon(y) = \frac{dV(y)}{dy} \]

\[ I_{DS} \cdot dy = W \mu C_{ox} \left[ (V_{GS} - V_T) - V(y) \right] dV(y) \]

\[ I_{DS} \int_0^L dy = W \mu C_{ox} \int_0^{V_{DS}} [V_{GS} - V_T - V(y)] dV(y) \]

\[ \therefore I_{DS} = \mu C_{ox} \left( \frac{W}{L} \right) \left[ (V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \]

\[ \beta = \beta' \left( \frac{W}{L} \right) \]
But that's not true as per experiments.

So what happens at 

\[ V_{gs} - V_T = V_{DS} \]

\( k \) beyond.

Saturation? 

\[ V_a - V_S \geq V_T \]
$I_{DS}$ & $V_{DS}$ relation is Parabolic

\[ \frac{\partial I_{DS}}{\partial V_{DS}} = \beta'(\frac{W}{L}) \left[ (V_{GS} - V_T) - V_{DS} \right] = 0 \]

\[ \therefore \text{Max occurs at } V_{DS} = V_{GS} - V_T \]
MOSFET I-V characteristics (Input)

Sub Threshold Region

NMOS Enhancement
MOS I-V characteristics (output)

\[ I_{DS} \]

\[ V_{CSn} \]

\[ V_G2 \]

\[ V_{CS1} \]

\[ V_G < V_T \]

\[ V_{DS} \]

\[ V_{OV} = V_{DS} \]

\[ V_A \] Early Voltage

\[ I_{DS} = \beta \left[ V_{OV} \cdot V_{OV} - \frac{1}{2} V_{OV}^2 \right] \]

\[ = \frac{1}{2} \beta V_{OV}^2 \]
MOS Transistor Model for Circuits

\[ I_{DS} = \mu C_{ox} \left( \frac{W}{L} \right) \left[ (V_{GS} - V_{T}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \]

\[ = \beta' \left( \frac{W}{L} \right) \left[ (V_{GS} - V_{T}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \]

\[ = \beta \left[ (V_{GS} - V_{T}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \]

Define \( V_{CS} - V_{T} = V_{GT} = V_{Exc} = V_{OV} \)

Then \( I_{DS} = \beta \left[ V_{OV} \cdot V_{DS} - \frac{1}{2} V_{DS}^2 \right] \)

\( V_{OV} > V_{DS} \)

\[ \rightarrow \text{Non-Saturation Mode} \]
(a) If \( V_{ov} > V_{Ds} \)
Channel exists throughout the Channel Length \( L \). Device is in Linear or Non-Saturation Mode. Device is like

(b) If \( V_{ov} \leq V_{Ds} \), Channel pinch-off occurs
Then
\[
I_{Ds} = \frac{1}{2} \beta \left[ V_{ov}^2 \right]
\]
Saturation Mode

\[ V_{Ds} \]
\[ V_{ov} \]
Sub Threshold

Saturation - Device as Current Source

Non-Saturation

\[ V_T \]
\[ V_{Ds} \]

Variable \( R \)
In Saturation:
Slope in $I_{DS}-V_{DS}$ characteristics means

$$I_{DS} \propto V_{DS}$$

$$I_{DS} = \frac{1}{2} \mu n C_{OX} \frac{W}{L} \left[ V_{ON} \right]^2 \left( 1 + \lambda V_{DS} \right)$$

where $\lambda$ is saturation parameter and is given by $\lambda = \frac{\chi'}{L}$

where $\chi' = \sqrt{\frac{2}{q N_{Substrate}}}$

$\therefore \lambda \propto \frac{1}{L}$

shorter channel length devices have larger $\lambda$
Hence Transistor is Modeled by Two Equations

\[ I_{DS} = \mu_n C_{ox} \left( \frac{W}{L} \right) \left[ (V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \]

\[ = \beta \left[ V_{OV} \cdot V_{DS} - \frac{1}{2} V_{DS}^2 \right] \quad \text{when} \quad V_{GS} - V_T > V_{DS} \]

i.e. Device is in Non Saturation Mode

And clearly if \( V_{DS} \) is small \( I_{DS} \propto V_{DS} \) i.e. Linear Mode

\[ \frac{\partial V_{DS}}{\partial I_{DS}} = \frac{1}{\beta (V_{GS} - V_T)} \Rightarrow \text{Resistive Behaviour} \]

which means for different values of \( V_{GS} \)

\[ R_{ON} = \frac{\partial V_{DS}}{\partial I_{DS}} \text{ varies inversely as } V_{GS} \text{ increases.} \]

Equivalent Circuit \( \equiv \) Non linear Resistor
In Saturation, with $\lambda$ Smaller

$$I_{DS} = \frac{1}{2} \beta \frac{V_{DS}}{V_{TH}}$$

$\neq f(V_{DS})$ : Device acts as

Constant current source which Voltage controlled source called $\text{VCCS}$

$$\Rightarrow \quad \text{VCCS}$$

An Amplifier (Voltage Amplifier here) can be represented as

$$\Delta V_{IN} \rightarrow \text{VCCS} \rightarrow \Delta I \rightarrow \text{Load} \rightarrow \Delta V_{OUT}$$

Gain = $\frac{\Delta V_{OUT}}{\Delta V_{IN}}$