Tuning LC oscillator

\[ C_{V_{\text{varactor}}} = \frac{g_0}{(1 + \frac{V_R}{\phi})^m} \]

\[ m = 0.4 \text{ to } 0.5 \]
Mathematical Model of VCO

\[ \phi = \frac{d\phi}{dt} \]

\[ \omega t = \phi \]
\[ \frac{d\phi}{dt} = \omega \]
\[ \phi = \int \omega \, dt + \phi_0 \]

In a VCO

\[ \omega_{\text{out}} = \omega_0 + K_{\text{VCO}} V_{\text{cont}} \]

We have oscillator output

\[ V_{\text{out}}(t) = V_m \cos \phi t = V_m \cos \int \omega_{\text{out}} \, dt + \phi_0 \]
\[ V_{out}(t) = V_m \cos \left\{ \omega t + KV_{eo} \int V_{cnt} \, dt + \phi_0 \right\} \]

Assume \( \phi_0 = 0 \)

If \( V_{cnt} \) is constant:
\[ V_{out}(t) = V_m \cos \left\{ \omega t + KV_{eo} \int V_m \cos \omega_m t \, dt \right\} \]

Then:
\[ V_{out}(t) = V_m \cos \left\{ \omega t + KV_{eo} \frac{V_m}{\omega_m} \sin \omega_m t \right\} \]

\[ = V_m \cos \omega t - \frac{KV_{eo} V_m}{2\omega_m} \left[ \cos (\omega_0-\omega_m)t - \cos (\omega_0+\omega_m)t \right] \]

Sideband:
\[ \omega_0 - \omega_m \quad \omega_0 \quad \omega_0 + \omega_m \]
Phase Lock Loop

PLL was invented in 1930

1. Locking VCO to a Frequency
2. Frequency Synthesizers
3. Used in Mobile phones, TV, Receivers, Pager, Telephony

- Digital PLL (b) Sinusoidal PLL 1965-1970
- Optical PLL 1965
Definition: A PLL is a Feedback system
That
Compares the Output Phase
With
The Input Phase.
Comparison is performed
By
PHASE COMPARATOR
Analog Designers find issues related to:

- Jitter
- Phase Noise

very difficult to handle at high frequencies, which are now used in most Electronic & Communication Systems. Even Digital Systems on Board (PCB) also get critically affected due to two parameters or characteristics as above.
Example: 100 MHz Pulse waveform (50% Duty Cycle), show period of 10 ps and alternating at 5 ps at every edge. But this is only an ideal case. Transitions normally do not occur at 5 ps edge and that creates what we term as Jitter.

\[ \text{Early Transition} \quad \text{Late Transitions} \]

- Ideal
- Non-Ideal
Jitter:

i. Deterministic
   - Cross talk
   - EMI radiation on Signal Path
   - Noise from Surroundings
   - Switching - Power Supply Droop
   - Ground Bounce

ii. Random:
   - Temperature, Process Variations,
     Interface States
   - Random Jitter is Gaussian in nature
   - Multiple random jitter sources add to RMS Jitter,
Phase Noise:
Variation in signal timings can also be represented in Frequency Domain and resultant Noise distribution is measured as Phase-Noise (PN).

\[
P_{\text{osc}}(f) = \begin{cases} 
\text{Power} & \text{for } f \approx f_0 \\
\text{1 Hz Bandwidth} & \text{for } f = f_0 + f_m
\end{cases}
\]

If PN is 0, then all oscillator Power goes to \(f_0\) but PN spread some power to adjacent frequencies, which results in Sidebands.
Phase Noise = \frac{\text{Power in 1 Hz Bandwidth at Offset freq}}{\text{Total Power of the Carrier}}
= \text{dBc/Hz}

[Diagram showing power versus frequency with labels: \(1/f\), \(1/f^2\), \(1/f^3\) noise, white frequency, flicker noise, \(\sqrt{\text{Th. Noise}}\).]
Terminology

Frequency Locked
Phase error < permissible phase error (e.g. 5% of the output freq.)

Pull-in range (Capture Range)
The frequency range over which a loop can acquire lock.

\[ \omega_{in} = (\omega_{FR} - \Delta(\theta)) \]

\[ \omega_{out} = (\omega_{FR}) \]
Terminology

**Jitter**:

- Deterministic.
- Random - specified in rms value or peak to peak.

**Cycle to cycle jitter.**

$$T + \Delta T_1 \quad T + \Delta T_2$$

**Accumulated jitter (cycle jitter).**

**Duty cycle distortion jitter.**
Basic IC PLL

Phase Detector

Definition of Phase detector

XOR gate as phase detector
Simple PLL

Phase detector output for different input skews
A Typical PLL in CMOS

- In (LC) Oscillator