Voltage References

1. Voltage Divider Reference
2. MOS VOLTAGE Reference
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1. Divider Reference with Resistors

\[
V_{\text{ref}} = \frac{R_2}{R_1 + R_2} V_{\text{DD}} = \frac{1}{1 + \frac{R_1}{R_2}} V_{\text{DD}}
\]

\[
\frac{dV_{\text{ref}}}{dV_{\text{DD}}} = \frac{R_2}{R_1 + R_2}
\]

\[
\frac{V_{\text{ref}}}{V_{\text{DD}}} \cdot \frac{dV_{\text{ref}}}{dV_{\text{DD}}} = \frac{R_1 + R_2}{R_2} \cdot \frac{R_2}{R_1 + R_2} = 1
\]

We see \( \frac{dV_{\text{ref}}}{V_{\text{ref}}} = \frac{dV_{\text{DD}}}{V_{\text{DD}}} \) [\% change in \( V_{\text{DD}} \) directly reflects in \% variation of \( V_{\text{ref}} \)]

\[
\therefore \quad T_{C_f}(V_{\text{ref}}) = \frac{1}{V_{\text{ref}}} \frac{dV_{\text{ref}}}{dT} = \frac{R_1}{R_2} \frac{V_{\text{ref}}}{V_{\text{DD}}} \left( \frac{1}{R_2} \frac{\partial R_2}{\partial T} - \frac{1}{R_1} \frac{\partial R_1}{\partial T} \right)
\]

\[
= \frac{R_1}{R_2} \frac{V_{\text{ref}}}{V_{\text{DD}}} \left[ T_{C_f}(R_2) - T_{C_f}(R_1) \right]
\]
Voltage Reference with MOSFET & Resistor

Clearly \( V_{GS} = V_{ref} \)

\[ I_{DS} = \frac{V_{DD} - V_{ref}}{R} \]

But \( I_{DS} = \frac{\beta}{2} (V_{ov})^2 \) for Transistor

\[ V_{DD} - V_{ref} = \frac{\beta}{2} R [V_{ref} - \frac{\beta}{2} R V_T]^2 \]

Solving

\[ V_{ref} = V_T + \sqrt{\frac{2}{\beta R} (V_{DD} - V_{ref})} \]

If \( V_{DD} \gg V_{ref} \)

Then \( V_{ref} = V_T + \sqrt{\frac{2}{\beta R} V_{DD}} \)
Then 

\[ \frac{S_{V_{\text{ref}}}}{V_{DD}} = \frac{V_{DD}}{V_{\text{ref}}} \cdot \frac{\partial V_{\text{ref}}}{\partial V_{DD}} \]

\[ = \frac{1}{V_{T} \cdot \sqrt{\frac{2\beta R}{V_{DD}}} + 2} \]

Further,

\[ T C_f (V_{\text{ref}}) = \frac{1}{V_{\text{ref}}} \cdot \frac{\partial V_{\text{ref}}}{\partial T} \]

\[ = \frac{1}{V_{\text{ref}}} \cdot \left[ V_{T} T C_f (V_{T}) - \frac{1}{2} \sqrt{\frac{2}{W/L}} \frac{V_{DD}}{R \beta'(T)} \cdot \left[ \frac{1}{T} \frac{\partial R}{\partial T} - \frac{1}{T} \right] \right] \]
Then \[ I_Q R = V_{TM} + \sqrt{\frac{2 \cdot 2 I_Q}{\beta_n'(W/L)_{1}}} \]

\[ \therefore (I_Q R - V_{TM})^2 = \frac{2 I_Q}{\beta_n'(W/L)_{1}} \]

\[ \Rightarrow I_Q^2 R^2 + V_{TM}^2 - 2 I_Q R V_{TM} = \frac{2 I_Q}{\beta_n'(W/L)_{1}} = 0 \]

One solution is

\[ \therefore I_Q = \frac{V_{TM}}{R} + \frac{1}{\beta_4 R^2} + \frac{1}{R} \sqrt{\frac{2 V_{TM}}{\beta_4 R} + \frac{1}{\beta_4^2 R^2}} \]

and other solution is

\[ I_Q = 0 \quad \text{giving} \quad I_1 = I_2 \]

This is trivial solution, but can occur in reality.
Since M3 & M4 are chosen to be identical (Same $\beta$ and $V_T$), with the mirror connected combination. \therefore I_1 = I_2, where $I_1$ flows from $V_{DD}$ to $V_{SS}$ (OV) through M5 and M1 and $I_2$ flows similarly from M4-M2 and through R. Clearly $V_{GS1} = I_2 \cdot R$ or $V_{GS1} = I_1 \cdot R$

But $V_{GS1} = V_{TN} + \sqrt{\frac{2I_1}{\beta'_n (W/L)_4}}$

\therefore $I_2R = I_1R = V_{TN} + \sqrt{\frac{2I_1}{\beta'_n (W/L)_4}}$

We define $I_1 = I_2 = I_{eq}$
A Better $V_T$ reference is possible using Bootstrap Technique.
In case of $I_1 = I_L = I_Q = 0$, we see that we need a Start-up Circuit.

Transistor M7 is 'ON' when initially Node ① is at '0' V. Thus M7 provides current to M1. This increases $V_{gs1}$ of M1, which in turn increases $I_2 (\frac{V_{gs1}}{R})$. By feedback (Common Source) action, Node ① voltage starts increasing ($V_{gs1} + V_{os2}$) and at one time $V_{gs}$ for M7 goes below $V_{T7}$, thereby shutting off M7. Here the Q point of Reference reaches second stable point. Further Starting Circuit then stops participating.
If \( R \) is created from polysilicon layer \((n^+)\), then \( TC_f(R) = \frac{1}{R} \left( \frac{dR}{dT} \right) = -2000 \text{ ppm/°C} \).

The \( \beta \)-multiplier circuit thus show

\[
TC_f(I_0) = -2 \times 2000 + \frac{1.5}{T(\text{ok})}
\]

\[
= +1000 \text{ ppm/°C} \quad \text{at} \quad T = 300^\circ \text{K}
\]

We can use this circuit as Voltage Reference \( V_{\text{ref}} \) equal to \( V_{\text{gs1}} \)

\[
V_{\text{ref}} = V_{\text{gs1}} = \frac{2}{\beta_1} R \left( 1 - \sqrt{\frac{1}{k}} \right) + V_{\text{tn}}
\]

\[
\frac{\partial V_{\text{ref}}}{\partial T} = \frac{\partial V_{\text{tn}}}{\partial T} + \frac{2}{\beta_1 R} \left( 1 - \sqrt{\frac{1}{k}} \right) \left[ \frac{1}{R} \frac{dR}{dT} + \frac{1}{\beta_1} \frac{\partial \beta_1}{\partial T} \right]
\]
\( \beta - \text{Multiplier VREF} \).

This scheme is also called Self-Biasing Scheme.

This also uses 'Starting Circuit' for Operation to begin.

\[ V_{DD} \]

\[ M3 \]

\[ I_{DS1} = I_0 \]

Here Width of \( M_2, W_2 \)

is chosen \( K \) times of Width \( W_1 \) of \( M_1 \)

\[ \alpha \ \beta_2 = K \ \beta_1 \]

Clearly \( V_{GS1} = V_{GS2} + I_0 R \)

\[ \alpha \ \sqrt{\frac{2I_0}{\beta_1}} = V_{TN} + \sqrt{\frac{2I_0}{K \beta_1}} + I_0 R \]

\[ \alpha \ I_0 = \frac{2}{R^2 \beta_1} \left( 1 - \frac{1}{\sqrt{K}} \right)^2 \]
We can find value of $K$, for $\frac{dV_{REF}}{dT} = 0$

Thus choice of $K$ can give $T_C (V_{REF}) = 0$

Corresponding

$$V_{REF} = V_{Th} + \frac{2}{R \beta_1} \left[ 1 - \frac{1}{\sqrt{K}} \right]$$
PTAT Current Biasing Scheme

As \( V_{GS1} = V_{GS2} \)
for same current in \( M1 \) & \( M2 \)

Also \( p_2 = k p_1 \) \((w_2 = k w_1)\)

\[ \therefore V_{GS1} = V_{GS2} = IR + V_{DS2} \] 

Diode currents are

\[ I_{D1} = I = I_{Sat} e^{\frac{Q V_{BE}}{K T n}} \]

\[ V_{BE} = V_{DS1} \]

\[ V_{DS1} = \frac{n k T}{q} \ln \frac{I}{I_{Sat}} \]

\[ V_{DS2} = \frac{n k T}{q} \ln \frac{I}{K \cdot I_{Sat}} \]
Substituting (2) in (1)

\[ \frac{n k T}{q} \ln \frac{I}{I_{sat}} = \frac{n k T}{q} \ln \frac{I}{k I_{sat}} + I R \]

\[ \frac{n k T}{q} \ln \left( \frac{I}{I_{sat}} \right) = IR \]

\[ \therefore \quad IR = \frac{n k T}{q} \ln K \]

\[ \therefore \quad I = \frac{n k T}{q R} \cdot \ln K \]

\[ n = 1 \quad \text{for Silicon diode in Active Mode (Diffusion) only} \]

\[ \therefore \quad I \propto T \quad (\text{Proportional to Absolute Temperature}) \]

\[ TC_f(I) \sim 1000 \text{ ppm/}^\circ C \]
Principle of Bandgap Reference

- Two quantities have opposite polarity $T_Cf$ and hence by adjustment of $K$ $T_Cf(V_{REF}) \to 0$
Bandgap Reference Circuit

To the PTAT circuit, we have additional resistance LR and Diode D3 in output arm. Then we get $V_{\text{Ref}}$ with noor

$$V_{\text{Ref}} = Tc_f(V_{\text{Ref}}) \rightarrow 0$$

From PTAT CRT

$$I = \frac{V_{\text{Thermal}}}{\ln(K)}$$

$V_{\text{Thermal}} = \frac{kT}{Q}$
Then \( V_{Ref} = V_{D3} + I \cdot L \cdot R \)

\[ = V_{D3} + \frac{L \cdot VT_{Thermal} \ln K}{1} \]

\[ V_{D3} = \frac{n k T}{q} \ln \frac{I}{K I_{Sat}} \]

\[ V_{Ref} = L \cdot VT_{THM} \cdot \ln K + VT_{THM} \ln \frac{I}{K I_{Sat}} \]

\[ = \ln \left[ \ln(K) + \ln \frac{I}{K I_{Sat}} \right] \]

For normal diode in CMOS Technology, with \( L = 12 \) \& \( K = 8 \) we get \( V_{Ref} = 1.25V \) (Bandgap of Silicon)

Further \( \frac{dV_{Ref}}{dT} \geq 0 \) value = value. If Adjust K, L is done