Lecture 32: Integrated circuit logic and packaging

1 Introduction

There are various elements that form part of an integrated circuit. Typical circuit elements include resistors (conductors), capacitors, diodes, and transistors. These can be divided into active and passive components. Active components are those that supply energy into the circuit and include transistors and diodes. Passive components do introduce energy into the circuit but
can only modify the introduced energy. Hence, they cannot amplify signals in the circuit. Passive components include resistors, capacitors, inductors, and transformers. The assembly of these different circuit elements defines the circuit microarchitecture. Very large scale integration (VLSI) circuit design deals with the assembly of these components to provide specific functionality. Packaging is the process that connects the assembled integrated circuit with the rest of the device. It defines the connections between the IC and external input/output elements, which form part of the device. Packaging is usually a series of steps, similar to IC fabrication, that makes these external connections. With decrease in device dimensions and increase in chip functionality, there are greater number of electrical connections that have to be made to the external circuit. This has also lead to a development in packaging technologies.

2 Silicon microarchitecture

Integrated circuits work on boolean logic, also called binary algebra or binary logic or boolean algebra. In boolean logic, there are only two states in the system, ON/OFF, TRUE/FALSE, high/low or 1/0. Consider a simple example, using numbers in the decimal system (base 10). These can be represented in the boolean algebra scheme using a combination of 1’s and 0’s. For example, the number 7 can be written as $4 + 2 + 1$, which can be rewritten as $1(2^2) + 1(2^1) + 1(2^0)$. Hence, the boolean representation for 7 is 111. Similarly, 6 would become 110 since $6 = 4 + 2 = 1(2^2) + 1(2^1) + 0(2^0)$. 8 cannot be written using 3 boolean symbols and needs 4 symbols. Thus, 8 would be 1000. Each 1 and 0 is called a bit. 8 bits make a byte. Thus, 6 and 7 can be represented by 3 bits, while 8 needs 4 bits.

It is possible to do arithmetic and logical operations using boolean algebra. Arithmetic operations include basic mathematical operations like addition, subtraction, multiplication, division and their offshoots. Logical operations (in the context of digital circuits) include AND, OR, NOT and variations like NAND, NOR, which are used for comparing two sets of data. These operations can be implement electronically using active and passive components of an IC.

2.1 OR logic gate

Consider the OR logical operation. As the name implies, the output of this operation is 1 (or ON) when either or both the inputs are 1 (ON). When both inputs are 0 (OFF), the output is also 0 (OFF). This can be represented in a
Table 1: Truth table for OR operation

<table>
<thead>
<tr>
<th>Input 1</th>
<th>Input 2</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
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<tr>
<td>1</td>
<td>0</td>
<td>1</td>
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<td>0</td>
<td>1</td>
<td>1</td>
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<tr>
<td>0</td>
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<td>0</td>
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</tbody>
</table>

Figure 1: OR gate made of (a) diodes or (b) transistors. This circuit can be fabricated using IC components by standard lithography techniques. Source [http://en.wikipedia.org/wiki/OR_gate](http://en.wikipedia.org/wiki/OR_gate)

The truth table, shown in table 1. It is possible to construct an OR gate, using common IC circuit elements. Figure 1 shows a OR gate, implemented using diodes or transistors. In both cases, the output will be high when either of the inputs are high.

2.2 AND logic gate

Another commonly used logic gate is the AND gate. In the AND gate, the output is ON, only when both inputs are ON. Else, the output is OFF. This can be represented in the truth table shown in table 2. Again, it is possible to represent the AND gate using diodes or transistors, as shown in figure 2. Similarly, other logic gates like NOT, NAND, NOR can be fabricated using
Table 2: Truth table for AND operation

<table>
<thead>
<tr>
<th>Input 1</th>
<th>Input 2</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
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<td>0</td>
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</tr>
</tbody>
</table>

Figure 2: AND gate made of (a) diodes and (b) transistors. This circuit can be implemented by standard lithography techniques. Source [http://en.wikipedia.org/wiki/OR_gate](http://en.wikipedia.org/wiki/OR_gate)
2.3 Memory elements

One of the important components of any IC is the presence of memory elements. These are usually random access memory (RAM) elements, which are used for storing data temporarily, so that it can be used for later operations and steps. It should be possible to read and write data to these memory elements. There are also read only memory (ROM) elements, which have longer data retention lifetimes, even in the absence of external power. Transistors can be used as memory elements, either static or dynamic elements. Dynamic memory elements can also be implemented using charge buildup with a capacitor, coupled with an access transistor. This is shown in figure 3.

Because the capacitor loses charge, the memory has to be constantly refreshed. Each memory element can store 1 bit, so an array of such memory elements are needed for storing data, depending on the no. of bits needed. Early computers were based on 16 bits, but now 32 and 64 bits are commonly used. There are also static memory elements, which do not need to be refreshed. They are implemented using several transistors and capacitors, as shown in figure 4. Another example of memory element is a floating gate.
Figure 4: Static RAM element implemented using a mixture of transistors and capacitors. Both reading and writing data to the RAM element is controlled by the transistors. Adapted from *Microchip fabrication* - Peter van Zant.
Figure 5: Floating gate MOSFET flash memory construction. There are two gates, one is a floating gate that stores the charge, while the control gate is used to write and read data to the memory element. Source http://product.tdk.com/en/techjournal/archives/vol01_ssd/contents03.html.

MOSFET, which is an example of a flash based memory. The working of a floating gate MOSFET is shown in figure 5. The MOSFET consists of two gates, one of which is electrically isolated, creating a floating node. This can be ‘written’ by the application of an electrical field to the gate, so that electrons can tunnel into this floating gate. Since, this gate is surrounded by a dielectric material with high resistance, the charge can be stored for a long time. When data is to be erased, an external reverse potential is applied to the gate. Floating gate MOSFETs are used for flash memories and programmable ROM (PROM). They are an example of a static memory device.

### 2.4 Microarchitecture

It is possible to build the different elements of a IC using the active and passive components, along with memory elements. Silicon microarchitecture refers to the global level of arrangement of these elements, to achieve specific functionality. Microprocessors are defined as circuits that combine both logic and memory elements. The elements perform specific logical/arithmetic operations on the incoming data, while the memory circuits are used to store and retrieve the data in different formats. The first practical microprocessor was introduced by Intel in 1972. This was a 4-bit processor. This means that integers and memory address were 4-bits long. Now, 64-bit processors are commonly used for personal computers. An Intel Pentium IV die is shown in figure 6. With decreasing transistor sizes, greater functionality can be packaged in ICs of the same area.
3 Packaging

The various components of the IC are connected to each other through the metallization layers. There are various levels in metallization, which provide different levels of connectivity (the latest Intel processors have 11 levels of metallization). The final metallization layer is used to connect the IC to external devices. Packaging refers to the set of processes that provide this electrical connectivity, thus allowing the chip to be integrated with other devices. Packaging is also used to provide physical protection to the chip. For a given system, the various components can be integrated into one chip. This is called System on Chip (SoC). There are also situations where multiple chips with specific functionality are integrated on a package, called System on Package (SoP).

There are various chip characteristics that affect the packaging process

1. Integration level
2. Wafer thickness
3. Chip dimensions
4. Environmental sensitivity - important for lead free packaging
5. Physical vulnerability
6. Heat generation
7. Heat sensitivity - heat generation and sensitivity are important during operation since adequate provision must be given for heat dissipation.

Usually, a passivation layer is grown on top of the wafer, at the end of the fabrication. This is provide for protection to the circuit elements. This passivation layer can be a hard layer (like silicon nitride or oxide) or a soft layer like polyimide. The electrical contacts are exposed, so that the chip can be connected to the system. There are four basic functions of a package

1. Substantial lead system - electrical connectivity
2. Physical protection
3. Environmental protection
4. Heat dissipation - this is very important for chips that are used in mobile computing, where active cooling elements cannot be implemented. Lower heat dissipation, by reduced power consumption, is also important for mobile computing since this save battery life.
Packaging is done after the wafers are done with the fabrication and sort process. The sort process isolates the dies that are good and need to be packaged. Packaging is a series of steps, similar to the assembly line process in fabrication, through which the dies pass before final inspection and delivery.

4 Packaging process

4.1 Backside prep

This is the first step in packaging, where the wafers are thinned. Typical 12” wafers, used in fabrication, have a thickness of 650-700 µm. This thickness is needed for wafer handling during fabrication, but less than 100 µm of Si is used. The thickness of the wafers can affect die separation and packaging and hence the wafers need to be thinned to approximately 100 µm. This is done by chemical mechanical polishing. The front side is protected during this process (using thick resist) to make sure no cracks or defects are introduced during thinning.

4.2 Die separation

The wafers are separated into individual dies. This is usually done by sawing or scribing the wafer, using a diamond saw or scribe, on pre patterned scribe lines. These scribe lines also have e-test structures, that are probed during sort, to identify the die yield. Scribe lines in a wafer are shown in figure 7.

4.3 Die pick and place

After die separation, the good dies are picked up for further processing. Prior to this, good/bad dies are identified in sort. The die sort, separation and pick process is shown in figure 8.

4.4 Die inspection

After die pick, the dies are inspected for cracks/defects on the good dies. This inspection is done using an optical microscope and the process is automated.

4.5 Die attach

After passing inspection, the die is then attached to the specific area of the package. An example is shown in figure 9. The die attach process is used to create a strong bond between the die and package and is the precursor for the
Figure 7: Scribe lines in a wafer separating individual dies. Some scribe lines also have e-test structures, which are used to test for electrical functionality before die separation. Scribe lines are also used during fabrication to test process quality. An expanded view of the e-test structure is shown in the bottom. Adapted from [http://www.lricks.com/wlrt.htm](http://www.lricks.com/wlrt.htm).

Figure 8: (a) A die sort process to identify good dies, (b) Separation of good dies, and (c) picking the good dies for further process. Bad dies are usually scrapped and the silicon reused. Adapted from *Microchip fabrication - Peter van Zant.*
wire and tape bonding process, during which electrical leads are attached. For the flip chip process, the die attach and bonding process are combined. The die attachment can be conductive e.g. using a gold-silicon eutectic. The eutectic has a melting point of 380 °C, shown in the phase diagram in figure 10. Hence, gold is plated on the bottom of the die, in contact with Si and then heated, so that the eutectic is formed and melts to form the bond. Non conducting attachments are also used. In this case, a epoxy adhesive material is used to attach the die to the package.

4.6 Bonding

Bonding is the most important step in the packaging process. In bonding, wires are connected to the leads in the IC, so that the IC is *electrically connected* with other devices. Bonding usually follows die attach, shown in figure 9 or the two steps are combined, as in the flip chip process. There are three main techniques for bonding

1. **Wire bonding** - this is carried out using gold or aluminum. The gold wire is fed through a capillary and by thermo mechanical compression is bonded with the die and lead. The schematic of this process is shown in figure 11. This type of bonding is also called *ball bonding*. In the case of Al, a wedge bond is formed between the die and the lead. This is

Figure 11: A gold wire bonding to the lead and die using a ball bonding. The gold wire is fed through the capillary and forms the bond with the lead on the package. Adapted from *Microchip fabrication - Peter van Zant.*
achieved by using ultrasonic vibration. The advantage of using Al is that, lower temperatures are needed and it is cheaper than gold. The Al wedge bond is shown in figure 12.

2. **Tape bonding** - tape bonding is used for extremely thin device fabrication. It is also called *tape automated bonding* (TAB). In this process, the electrical lead system is deposited on a flexible tape by sputtering or thermal evaporation. This is combined with a patterning or stamping process to make the leads on the tape. For bonding, the die is position and aligned with the leads on the tape and the bonding is completed by a tool called the *thermode*. The thermode has a heated flat diamond surface that forces the tape onto the die and makes the bond. The process is shown in figure 13.

3. **Flip-chip bonding** - this is also called *bump and ball bonding* or *controlled collapse chip connection* (C4). It is currently in use in the IC industry, due to the large number of leads and the small spacing between them. In this process, the wires are replaced by a reflowed solder bump, as shown in figure 14. The metal bumps are deposited on top of the leads on the die and the chip is then flipped (hence the name
Figure 13: Schematic of the tape bonding process. This is used for thin device fabrication where leads are deposited on a flexible tape, patterned, and then stamped on the pads. Adapted from *Microchip fabrication* - Peter van Zant.

Figure 14: Reflowed solder bump that is used for flip-chip bonding. These are locally deposited on the leads and the chip is bonded to these directly without any wires. Adapted from *Microchip fabrication* - Peter van Zant.
Figure 15: Schematic of the Flip-chip or C4 bonding process in (a) plan view and (b) cross section. The solder is flowed on to leads on the substrate and then the chip is flipped and the leads on the chip are attached to the substrate through the solder. Thus, both die attach and bonding are combined in one step. Adapted from *Microchip fabrication* - Peter van Zant.

flip chip) and bonded with the package using the solder bumps. The process is shown in figure 15. There is no separate die attach step, since both attach and bonding takes place through the solder bumps. For additional mechanical stability, an epoxy filling is also used. The formation of the reflow solder process takes place partly in the fab, through a series of processing steps. These steps are summarized in figure 16. Some of the steps are carried out during fabrication, in the back end process.

### 4.7 Pre seal inspection

After bonding, there is an inspection step to check the bonds formed. This inspection uses optical measurements, to check the bonding and reliability measurements for checking the electrical connectivity. There are different reliability criteria depending on the nature of the application.

### 4.8 Sealing

After inspection, the die is sealed in a protective enclosure. Seals can be hermetic or non-hermetic, depending on the application. Hermetic seals help in isolating the die from the atmosphere and include welding, soldering, and glass sealing. Non hermetic seals use epoxy molding, while hermetic
seals are usually premade packages, either with ceramic or low melting glass (CERDIP). The parts of the CERDIP package are shown in figure 17.

4.9 Final steps

Once the die is sealed, the leads are coated with lead-tin solder. This is to help in bonding the package to a printed circuit board. It also helps in proving the electrical connectivity with other devices. This process is called lead plating. Then the excess lead is removed, a process called lead trimming. Then, the package is marked, package marking, and then the final step is electrical testing, appropriately called final testing. Packages that pass final testing are then sent for assembly or shipped to the customer.
Figure 17: (a) Top and (b) bottom part of the CERDIP package. The top part has a cavity where the die sits and it is coated with low melting glass to form a hermetic seal. The bottom part contains the die with all the electrical leads attached. Adapted from *Microchip fabrication* - Peter van Zant.