“PACKAGES” (CONTINUED)
Multi Chip Modules (MCM) or Multi chip packaging

- Industry’s first MCM from IBM.
- Generally MCMs are horizontal or two-dimensional modules.

Defined as a single unit containing two or more chips and an interconnection substrate which function together as a system building block.

Need for MCM

- More functionality in one ‘single chip’
- Special circuit needs met
- MCMs formed from multiple chips on a common substrate / package structure
- Do away with individually packaged chips on a PWB

Figure Source: Prof Rao R Tummala, PRC, GTech.
Multiple Chip Module (MCM)

- Increase integration level of system (smaller size)
- Decrease loading of external signals, hence, higher electrical performance
- No packaging of individual chips
- Problems with cooling; special cooling requirements may be required yet
- Still expensive; but used for high-end applications (e.g., military, aerospace etc); a complete PC in a MCM possible

Figure Source: Wikimedia Commons
Type of MCMs
1. MCM-Deposited thin film
2. MCM-Ceramic
3. MCM-Laminated organic

What are the issues?
1. Feature size
2. Via size
3. Layer count
4. Dielectric constant
5. Dielectric thickness
6. Integrated resistors/capacitors $R, C$

Figure Source: Fundamentals of MSP- Rao Tummala
Multichip Module: MCM-L

Organic substrates-based MCM-L
Based on laminated PCB technologies and using microvias, that have evolved to accomplish the denser integration requirements of today’s demands.

Comparison with MCM-C and MCM-D
Low cost.
Parallel fabrication process
Ease of repairing of reworking individual layers
Well-established infrastructure; based on PWB manufacturing
Assemblies with components in both sides

Drawback:
Significant CTE mismatch between substrate and die materials
Low performance and wiring density
Poor thermal conductivity of substrate
Moisture sensitivity of materials
High Crosstalk noise
Ceramic substrate-based MCM-C
Substrates based on co-fired ceramic or glass-ceramic technologies.

Comparison with MCM-L and MCM-D
High wiring density
Better electrical and thermal conductivity than MCM-L
Assemblies with components on both sides
Flexible packaging
Superior strength and rigidity
Parallel manufacturing process
Lower wiring density than MCM-D
High dielectric constant (not suitable for high frequencies)

Figure Source: Fundamentals of MSP- Rao Tummala
Multichip Module: MCM-D

Silicon substrate-based MCM-D
MCM-D are formed by Deposited dielectrics and conductors on a base substrate typically made with silicon.

Comparison with MCM-L and MCM-C
- Highest performance
- Highest wiring density
- Low dielectric constant
- Good electrical properties
- Highest cost

MCM-L : MCM-C : MCM-D

1 5 10
System in Package is defined as the vertical stacking of similar or dissimilar ICs, in contrast to the horizontal nature of SOC.

Benefits: simpler design, design verification and process besides minimal time-to-market.

About 30 IC and packaging companies are producing SIP-based multichip modules.

SiP is a key technology for reducing product size and increasing product functionality in products like digital cameras and mobile phones.

Figure Source: Fundamentals of MSP- Rao Tummala
SiP may contain one or more IC chips (wire bonded or flip chip) plus other components that are traditionally found on the system mother board such as:

- **Passive Components:**
  - Surface mount discrete passive ✔
  - Integrated passive networks (IPNs) ✔
  - Passives embedded or patterned in the package substrate

Other typical components assembled on the system board:
- SAW / BAW filters
- EMI Shields
- Pre-packaged ICs
- Connectors
- Mechanical parts

The power of SiP is the ability to bring together many IC and package assembly and test technologies to create highly integrated products with optimized cost, size and performance.
System-on-Package

1. Seamless integration of functional Units (chips)
2. A single-level packaged system

Figure Source: Prof. Rao Tummala, GTech
Current Trends

• 3D Packaging- Stacked Die
• Build-Up Substrates (organic)
• Flip-Chip
  – DCA- Direct Chip Attach
• SiP
  – LTCC, Bluetooth Standard
• “Green” Manufacturing
  – Removing Lead (Pb)
  – New Materials (tin, silver, copper)
    for Die Attach, plating, solder balls
• SOP, POP (package-on-package)

Figure Source: Wikimedia Commons
## Road Map for Hand Held Devices

### Table: Metrics and Yearly Progress

<table>
<thead>
<tr>
<th>First Year of Significant Production</th>
<th>Metric</th>
<th>2003</th>
<th>2005</th>
<th>2007</th>
<th>2013</th>
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<tbody>
<tr>
<td>Board Assembly (Conversion) Cost</td>
<td>$ per I/O</td>
<td>0.5</td>
<td>0.45</td>
<td>0.4</td>
<td>0.3</td>
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<tr>
<td>Package I/O Pitch (Perimeter)</td>
<td>mm</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
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<tr>
<td>Package I/O Pitch (Area Array)</td>
<td>mm</td>
<td>0.5</td>
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<td>0.5</td>
<td>0.5</td>
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<tr>
<td>Substrate Lines and Spaces</td>
<td>microns</td>
<td>75</td>
<td>65</td>
<td>65</td>
<td>35</td>
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<tr>
<td>Substrate Pad Diameter*</td>
<td>microns</td>
<td>225</td>
<td>200</td>
<td>175</td>
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### Table: Solder and Component Progress

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<tr>
<th>Solder</th>
<th>Composition</th>
<th>Lead / Lead-Free</th>
<th>Lead-Free / Lead</th>
<th>Lead-Free</th>
<th>Lead-Free</th>
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<td>RF Components Thickness</td>
<td>mm</td>
<td>2.5</td>
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<td>1.5, MEMS</td>
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<td>Passive Components</td>
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<td>Embedded</td>
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<td>Product Introduction Cycle</td>
<td>Months</td>
<td>10</td>
<td>9</td>
<td>8</td>
<td>6</td>
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<tr>
<td>Time, Platform</td>
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<tr>
<td>Product Introduction Cycle</td>
<td>Months</td>
<td>4</td>
<td>3</td>
<td>2</td>
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<td>Time, Spin</td>
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*Figure Source: INEMI*
## Business Systems: Board Assembly

### First Year of Significant Production:

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<tbody>
<tr>
<td>Board Assembly (Conversion) Cost</td>
<td>$/I/O</td>
<td>0.8</td>
<td>0.75</td>
<td>0.7</td>
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<tr>
<td>Substrate Cost (14 layer, no blind/buried)</td>
<td>$/cm²</td>
<td>0.14</td>
<td>0.13</td>
<td>0.12</td>
<td>0.11</td>
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<tr>
<td>(28 layer, blind &amp; buried vas)</td>
<td>$/cm²</td>
<td>0.45</td>
<td>0.43</td>
<td>0.41</td>
<td>0.39</td>
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<td>(48 layer, blind &amp; buried vas)</td>
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<td>Package I/O Pitch (perimeter)</td>
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<td>0.35</td>
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<tr>
<td>Max I/O Density (area array)</td>
<td>I/O/cm²</td>
<td>237</td>
<td>256</td>
<td>278</td>
<td>331</td>
<td>400</td>
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<tr>
<td>Max I/O Density (perimeter)</td>
<td>I/O/cm²</td>
<td>48</td>
<td>56</td>
<td>58</td>
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<tr>
<td>Substrate Lines/Space (laminate)</td>
<td>μm</td>
<td>55/75</td>
<td>50/70</td>
<td>45/65</td>
<td>40/60</td>
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<tr>
<td>Thin Film Lines/Space</td>
<td>μm</td>
<td>8/16</td>
<td>6/12</td>
<td>6/11</td>
<td>5/11</td>
<td>5/10</td>
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<tr>
<td>Substrate Pad Diameter</td>
<td>μm</td>
<td>325</td>
<td>300</td>
<td>280</td>
<td>250</td>
<td>200</td>
</tr>
</tbody>
</table>

*Figure Source: INEMI*
SUMMARY

• PGAs to BGAs
• Peripheral array to area array packaging
• Conventional package footprint to CSP
• Single chip package to multi chip packaging
• Packaged chips to flip chip direct chip attach, FC-DCA
• Mechanically drilled vias to microvias by various technologies (laser)
• Closer integration of packaging hierarchies
• Environmental aspects in production taken care of
• Time to volume times drastically reduced
Hybrid Circuit is one in which either the **bare die** or **a packaged die** is mounted on a ceramic substrate and interconnected to **on-board passives**.

Two types of hybrids are known depending on the technology used to build the discrete passives components:

1. - Thick Film Hybrids
2. - Thin Film Hybrids
Thick Film Hybrids
Print and fire technology

“Inks” are used to make conductors, resistors, capacitors. Desired properties are obtained ONLY AFTER “FIRING”.

- Conducting Inks – For Tracks
- Resistor Inks - Resistors - trimmed
- Dielectric Inks – To build Capacitors
- Substrate - Co-fired ceramics
Vacuum deposition techniques are used to deposit conductors, resistors and dielectrics to build the passive components followed by laser trimming to obtain precise values.

**Thin Film Hybrids**

Vacuum deposition technology

**HTCC** - High temperature Co-fired Ceramics

[750°C to 1000°C]

**LTCC** - Low temperature Co-fired Ceramics

[350°C to 600°C]
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