EE669: VLSI TECHNOLOGY
Autumn Semester Graduate Course
2014-2015 Session
by

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Course Syllabus

Examination Schedules

Autumn Semester Exam Dates:
Quiz/Cum Test : 4th Week in August 2014
Test -1 : 2nd Week in October 2014
Mid-Semester Exam: September 2014 (Institute Time table or as decided by us)
End-Semester Exam: Mid- November 2014

All Examinations except Mid-semester and End semester ones will be from 8.45 to 10.45 PM slot in GG 001 and GG 002

Home assignments/Project submission as per announced dates, time to time.
Grading Policy:

Total of 4 Exams:
- Quiz, Test, Mid-Semester and End-Semester
  Weightage in %: \(8 + 8 + 20 + 50 = 86\)

AND some Design Project/Problem Assignments
  Weightage: = 15\%

PLUS 7 \% Total bonus on
  Attendance (80 \% Min), Sincerity, Project preparation and excellence in Exams.

TOTAL : 100 \% (108 in actual number)
History of Electronic Devices

1900: Vacuum tube
1930: Triode, Diode
20th century:
- 1st Electronic circuits
- Solid-State Circuits

- 20 years
- 30 years
- 10 years

- MOSFET
- MISFET
- 1st Transistor
- Transistor Concept

Late 20th century:
- MOSFET
- Si-MOSFET
- IC
- LSI
- VLSI
- ULSI

- Low Power
- High speed
- High integration
- High reliability
- Low Power
1906: Vacuum Tube: Triode

Lee De Forest

Iwai Hiroshi
J. E. LILIENFELD

DEVICES FOR CONTROLLED ELECTRIC CURRENT

Filed March 28, 1928

J. E. LILIENFELD

Patented Mar. 7, 1933

1,900,018

UNITED STATES PATENT OFFICE

JULIUS EDGAR LILIENFELD, OF BROOKLYN, NEW YORK
DEVICE FOR CONTROLLING ELECTRIC CURRENT

J. E. LILIENFELD
DEVICE FOR CONTROLLING ELECTRIC CURRENT
Filed March 28, 1928
1947: 1st transistor

J. Bardeen, W. Bratten, W. Shockley
First Bipolar Ge Transistor
1958: 1st Integrated Circuit

Jack S. Kilby

Iwai Hiroshi
1958 - Integrated circuit invented

September 12th 1958 Jack Kilby at Texas instrument had built a simple oscillator IC with five integrated components (resistors, capacitors, distributed capacitors and transistors).

In 2000 the importance of the IC was recognized when Kilby shared the Nobel prize in physics with two others. Kilby was sited by the Nobel committee "for his part in the invention of the integrated circuit a simple oscillator IC"
1959: 1st Planar Integrated Circuit

Robert N. Noyce
1960: First MOSFET by D. Kahng and M. Atalla

Top View

Si
Source
Drain
Al Gate

Si/SiO2 Interface is extraordinarily good
First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

Today's pocket PC made of semiconductor has much higher performance with extremely low power consumption
1970,71: 1st generation of LSIs

DRAM  Intel 1103

MPU   Intel 4004
In 2012

Most Recent SD Card

128GB (Byte)
= 128G X 8bit
= 1T (Tera) bit

1T = 1012 = 1 Trillion

World Population : 7 Billion
Brain Cell : 10 ~ 100 Billion
Stars in Galaxy : 100 Billion

Iwai Hiroshi
128 GB = 1Tbit

2.4cm × 3.2cm × 0.21cm

Volume : 1.6 cm³  Weight : 2g

Voltage : 2.7 - 3.6V

Old Vacuum Tube :
5cm X 5cm X 10cm, 100g, 50W

What are volume, weight, power consumption for 1Tbit

Iwai Hiroshi
Old Vacuum Tube:
5cm X 5cm X 10cm

1Tbit = 10,000 X 10,000 X 10,000 bit
Volume = (5cm X 10,000) X (5cm X 10,000) X (10cm X 10,000)
= 0.5km X 0.5km X 1km

Pingan International Finance Center
Shanghai, China (Year 2016)
700 m

Indian Tower
Mumbai, India (Year 2016)
700 m

Burj Khalifa
Dubai, UAE (Year 2010)
828 m

500 m

1Tbit
Old Vacuum Tube: 50W

Nuclear Power Generator
1MkW = 1BW

1Tbit = 1012bit

Power = 0.05kWX1012 = 50 TW

We need **50,000 Nuclear Power Plant** for just one 128 GB memory

In Japan we have only **54 Nuclear Power Generator**

Last summer **Tokyo Electric Power Company (TEPCO)** can supply only 55BW.

We need 1000 TEPCO just one 128 GB memory

Imagine how many memories are used in the world!
So progress of integrated circuits is extremely important for power saving.
Brain: Integrated Circuits

Ear, Eye : Sensor

Mouth : RF/Opto device

Stomach : PV device

Hands, Legs : Power device

Iwai Hiroshi
Near future smart-society has to treat huge data.

Demand to high-performance and low power CMOS become much more stronger.
Semiconductor Device Market will grow 5 times in 12 years, even though, it is very matured market!!

2011
300B USD

→

2025
1,500B USD

Gartner: By K. Kim, CSTIC 2012
1970, 71: 1st generation of LSIs

DRAM   Intel 1103

MPU    Intel 4004
Cost of chip production

- At 1000 wafers/month (lots of parts!)
  - ~$600/6 inch 0.25u wafer=~$3.50/cm²
  - Add for packaging ~0.25 cents/pin for QFP
    (about most expensive)
  - Add for testing $200/hour for 256 pin mixed signal tester; about 1 second to move sites
- (6 inch wafer ~ 180 cm², 8 inch ~ 310 cm²)

From numbers like these, you can compute production price of your chip

Thanks to Chuck Neugebauer for prices ca. 2005
Today, silicon device is the indispensable and most important devices for our human society. Everything has to be controlled by Si device.

Si realized extremely high-frequency (speed) operation with extremely low cost, low power, small size, high reliability.

Today’s IT -- such as internet, i-mode, cellular phone, GPS navigation, game machine, Entertainment robot – could not be realized Without Si integrated circuit development.
Introduction: microelectronics vs. nanoelectronics
1900 “Electronics” started.

Device: Vacuum tube

Device feature size: Several cm

Major Appl.: Amplifier (Radio, TV, Wireless etc.)

→ Technology Revolution

1970 “Micro-Electronics” started.

Device: Si MOS integrated circuits

Device feature size: 10 µm

Major Appl.: Digital (Computer, PC, etc.)

→ Technology Revolution
2000 “Nano-Electronics” started.

Device: Still, Si CMOS integrated circuits

Device feature size: 100 nm

Major Appl.: Digital (µ-processor, cell phone, etc.)

→ Technology Revolution??

Maybe, just evolution and innovation!

But great evolution or innovations!

and so many innovations!
Now, 2014 “Nano-Electronics” continued.

Device: Still, Si CMOS integrated circuits

Device feature size: around 10 nm

Major Appl.: Still Digital (µ-processor, cell phone, etc.)

Still evolution and innovation.
Goal: 1TIPS by 2010

How do you get there?

INTEL
Technology has scaled well, will it in the future?

- Dimensions scale down by 30%
- Oxide thickness scales down
- Vdd & Vt scaling
- Doubles transistor density
- Faster transistor, higher performance
- Lower active power
Scaling Evolution

Downsizing of the components has been the driving force for circuit evolution

<table>
<thead>
<tr>
<th>Year</th>
<th>Component</th>
</tr>
</thead>
<tbody>
<tr>
<td>1900</td>
<td>Vacuum Tube</td>
</tr>
<tr>
<td>1950</td>
<td>Transistor</td>
</tr>
<tr>
<td>1960</td>
<td>IC</td>
</tr>
<tr>
<td>1970</td>
<td>LSI</td>
</tr>
<tr>
<td>2000</td>
<td>ULSI</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Feature Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 cm</td>
</tr>
<tr>
<td>10^{-1}m</td>
</tr>
<tr>
<td>10 cm</td>
</tr>
<tr>
<td>10^{-2}m</td>
</tr>
<tr>
<td>mm</td>
</tr>
<tr>
<td>10^{-3}m</td>
</tr>
<tr>
<td>10 \mu m</td>
</tr>
<tr>
<td>10^{-5}m</td>
</tr>
<tr>
<td>100 nm</td>
</tr>
<tr>
<td>10^{-7}m</td>
</tr>
</tbody>
</table>

In 100 years, the feature size reduced by one million times

Clock Frequency (GHz)

Production Year

![Graph showing clock frequency over time with various data points and trend lines.]

Iwai Hiroshi
Integrated circuit evolution:

1960s

Integrated circuit evolution:

Early 1990s

Progress due to:

- feature size reduction: 0.7X every 3 years (Moore's Law)
- increasing chip size ~ 16% increase in area per year
- innovations in implementing functions and in process technology

J.L. Hoyt
MIT
Scaling:

Importance of Downsizing

- Capacitance reduction → Power reduction
- High integration → Speed increase
- Function increase
- Parallel processing → Speed increase

Iwai Hiroshi
Demand for future VLSI:

Much higher performance
Much lower power consumption

Thus, downsizing of Si devices is the most important and critical issue.


## Prediction of Scaling limit

Vacuum tube era : even μm size could not be imagined
Since Si IC started

<table>
<thead>
<tr>
<th>Period</th>
<th>Expected limit(size)</th>
<th>Cause</th>
</tr>
</thead>
<tbody>
<tr>
<td>Late 1970’s</td>
<td>1μm:</td>
<td>SCE</td>
</tr>
<tr>
<td>Early 1980’s</td>
<td>0.5μm:</td>
<td>S/D resistance</td>
</tr>
<tr>
<td>Early 1980’s</td>
<td>0.25μm:</td>
<td>Direct-tunneling of gate SiO2</td>
</tr>
<tr>
<td>Late 1980’s</td>
<td>0.1μm:</td>
<td>‘0.1μm brick wall’ (various)</td>
</tr>
<tr>
<td>Today</td>
<td>50nm:</td>
<td>‘Red brick wall’ (various)</td>
</tr>
<tr>
<td>Today</td>
<td>10nm:</td>
<td>Fundamental?</td>
</tr>
</tbody>
</table>
On track for 1B transistor integration capacity
Exponential growth: number of transistors on a chip doubles in a certain period (e.g. every 18 months, in 1980's)

Limits of Moore’s Law?

- Growth expected until 30 nm gate length (currently: 180 nm)
  - size halved every 18 mos. - reached in
    - $2001 + 1.5 \log_2((180/30)^2) = 2009$
  - what then?

- Paradigm shift needed in fabrication process
Technological Background of the Moore’s Law

• To accommodate this change, the size of the silicon wafers on which the integrated circuits are fabricated have also increased by a very significant factor – from the 2 and 3 in diameter wafers to the 8 in (200 mm) and 12 in (300 mm) diameter wafers

• The latest catch phrase in semiconductor technology (as well as in other material science) is nanotechnology – usually referring to GaAs devices based on quantum mechanical phenomena

• These devices have feature size (such as film thickness, line width etc) measured in nanometres or 10-9 metres
Recurring Costs

Variable Cost = \( \frac{\text{Cost of (Die + Die test + packaging)}}{\text{Final Test Yield}} \)

Cost of Die = \( \frac{\text{Cost of wafer}}{\text{Dies per wafer} \times \text{Die Yield}} \)

\[ \frac{\pi \times \text{wafer diameter}^2}{\text{Die area}} = \frac{\pi \times \text{wafer diameter}}{1.414 \times \text{Die area}} \]

Die yield = \[ 1 + \frac{\text{defects per unit area} \times \text{Die area}}{\alpha} \] – \( \alpha \)
Yield Example

- Example
  
  wafer size of 12 inches, die size of 2.5 cm², 1 defects/cm², \( \alpha = 3 \) (measure of manufacturing process complexity)
  
  252 dies/wafer (remember, wafers round & dies square)
  
  die yield of 16%
  
  \[ 252 \times 16\% = \text{only 40 dies/wafer die yield!} \]

- Die cost is strong function of die area
  - proportional to the third or fourth power of the die area
Transistors and Memories

- 3 different insulators
- Gate
- Transistor
- High stress film
- n-type MOSFET
- Source
- Drain
- Capacitors
- Transistors
- Floating Gate
- Control Gate
- DRAM
- Flash Memory
A Simple nMOS Fabrication

(a) photoresist
(b) B field implant
(c) B channel implant
(d) poly-silicon gate
(e) Arsenic implant
(f) source n⁺ drain
(g) p-Si <100>
(h) Gate Drain Source L_g
PROCESS STEPS

- Chemical Vapor Deposition and Oxidation
  - Insulating dielectrics
- Lithography
  - Optical techniques for patterning photoresists
- Physical Vapor Deposition
  - Vacuum techniques for evaporation and sputtering of metals and other materials
- Wet and Dry Etching
  - Pattern transfer techniques
- Diffusion, Implantation and Annealing
  - Material modification techniques
- Characterization
  - Optical, other, and electrical measurements during and following processing
Is Transistor a Good Switch?

On

$I = \infty$

$I = 0$

$\text{Sub-threshold Leakage}$

Off

$I = 0$

$I = 0$

$I = 1 \text{ma/u}$