

Questions for self assessment

Module 1--Lecture 1

1. What is the typical number of transistors to consider a circuit as VLSI?
2. Discuss the basic VLSI design flow using an example.
3. Why is verification necessary at each step of the design flow?

Module 1--Lecture 2

1. What are HDLs? Give some examples of HDLs.
2. What is CDFG? Why is CDFG considered to be suitable for modeling a circuit (HDL)?
3. Draw the CDFs for “while” and “if-then-else” statements in Verilog.
4. For what cases timing in CDFG required?
5. CDFGs can be represented as “Control flow based representation” or “Data flow based representation”. Explain the pros and cons of each of the representations.

Module 1--Lecture 3

1. Describe some basic transformations that can be performed on CDFGs.
2. Explain with examples the different types of compiler based transformations.
3. Explain with examples the different types of flow-graph based transformations.
4. Why do we say, “For hardware library based transformation, knowledge of design library is mandatory”?
5. Among all the transformations discussed in this lecture, which one do you feel has the maximum impact?