## Advanced VLSI Design - Video course

### COURSE OUTLINE

Historical Perspective of VLSI, CMOS VLSI Design for Power and Speed consideration, Logical Efforts: Designing Fast CMOS Circuits; Datapath Design, Interconnect aware design, Hardware Description Languages for VLSI Design, FSM Controller/Datapath and Processor Design, VLSI Design Automation, and VLSI Design Test and Verification.

### COURSE DETAIL

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<th>Module</th>
<th>Lecture Topics</th>
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| 1: CMOS VLSI Design for Power and Speed consideration (Prof. A.N.Chandorkar) | 1. Historical Perspective and Future Trends in CMOS VLSI Circuit and System Design- Part-I  
2. Historical Perspective and Future Trends in CMOS VLSI Circuit and System Design - Part II  
3. Logical Effort - A way of Designing Fast CMOS Circuits  
4. Logical Effort - A way of Designing Fast CMOS Circuits -Part II  
5. Logical Effort - A way of Designing Fast CMOS Circuits -Part III  
6. Power Estimation and Control in CMOS VLSI circuits  
7. Power Estimation and Control in CMOS VLSI circuits -Part II  
8. Low Power Design Techniques- Part-I  
9. Low Power Design Techniques -Part II |

### Pre-requisites:
- Basic course on VLSI Design

### Additional Reading:
- Technical Papers in following Journals:  

### Coordinators:
- Prof. A.N. Chandorkar  
  Department of Electrical EngineeringIIT Bombay  
- Prof. Dinesh Sharma  
  Department of Electrical Engineering
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<th>Section</th>
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| 2       | Datapath Design (Prof. A.N.Chandorkar)                               | 11. Arithmetic Implementation Strategies for VLSI – Part I  
12. Arithmetic Implementation Strategies for VLSI -Part II  
13. Arithmetic Implementation Strategies for VLSI -Part III  
14. Arithmetic Implementation Strategies for VLSI -Part IV |
| 3       | Interconnect aware design (Prof. Dinesh Sharma)                     | 15. Interconnect aware design: Impact of scaling, buffer insertion and Inductive peaking  
16. Interconnect aware design: Low swing and Current mode signaling  
17. Interconnect aware design: Capacitively coupled interconnects |
| 4       | Hardware Description Languages for VLSI Design (Prof. Dinesh Sharma) | 18. Managing concurrency and time in Hardware Description Languages  
19. Introduction to VHDL  
20. Basic Components in VHDL  
21. Structural Description in VHDL  
22. Behavioral Description in VHDL  
23. Introduction to Verilog |
| 5       | FSM Controller/Datapath and Processor Design (Prof. Sachin Patkar)   | 24. FSM + datapath (GCD example)  
25. FSM + datapath (continued)  
26. Single Cycle MMIPS  
27. Multicycle MMIPS  
28. Multicycle MMIPS – FSM |
| 6       | VLSI Design Automation (Prof. Sachin Patkar)                        | 29. Brief Overview of Basic VLSI Design Automation Concepts  
30. Netlist and System Partitioning  
31. Timing Analysis in the context of Physical Design Automation |
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<th>7: VLSI Design Test and Verification (Prof. Virendra Singh)</th>
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<td>33. Introduction to VLSI Testing</td>
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<td>34. VLSI Test Basics - I</td>
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<td>36. VLSI Testing: Automatic Test Pattern Generation</td>
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<td>37. VLSI Testing: Design for Test (DFT)</td>
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<td>38. VLSI Testing: Built-In Self-Test (BIST)</td>
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<td>39. VLSI Design Verification: An Introduction</td>
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<td>40. VLSI Design Verification: Equivalence Checking</td>
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<td>41. VLSI Design Verification: Equivalence/Model Checking</td>
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<td>42. VLSI Design Verification: Model Checking</td>
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References:


- **Module 6**: “VLSI Physical Design: From Graph Partitioning to Timing Closure”, Kahng and Lienig, Springer, 2011

- **Module 7**: “Essential of Electronic Testing for Digital, Memory, and Mixed Signal VLSI Circuits”, M.L. Bushnell