CMOS DIGITAL VLSI DESIGN

PROF. SUDEB DASGUPTA
Department of Electronics & Communication Engineering
IIT Roorkee

TYPE OF COURSE: Rerun | Elective | UG/PG
COURSE DURATION: 8 weeks (18 Jan' 21 - 12 Mar' 21)
EXAM DATE: 21 Mar 2021

PRE-REQUISITES: A basic course of Semiconductor Devices and Digital Electronics. A course on Computer Organization will be quite helpful.

INTENDED AUDIENCE: Final year Undergraduates and/or First year Master Student (Microelectronics)
INDUSTRIES APPLICABLE TO: Cadence, Synopsys, ST Microelectronics, NXP Semiconductors, SCL, Chandigarh

COURSE OUTLINE:
This course brings circuit and system level views on design on the same platform. The course starts with basic device understanding and then deals with complex digital circuits keeping in mind the current trend in technology. The course follows a design perspective, starts from basic specifications and ends with system level blocks. Eight Assignments are provided which will add/help in understanding the course in a better manner both at conceptual as well as hands-on level.

ABOUT INSTRUCTOR:
Prof. S. Dasgupta is presently working as an Associate Professor, in Microelectronics and VLSI Group of the Department of Electronics and Communication Engineering at Indian Institute of Technology, Roorkee. He received his PhD degree in Electronics Engineering from Institute of Technology-Banaras Hindu University (currently IIT-BHU), Varanasi in 2000. During his PhD work, he carried out research in the area of effects of ionizing radiation on MOSFET. Subsequently, he was member of faculty of Department of Electronics Engg., at Indian School of Mines, Dhanbad (currently IIT-Dhanbad). In 2006, he joined as an Assistant Professor in the Department of Electronics and Communication Engineering at Indian Institute of Technology, Roorkee. He is currently the Chairman, Faculty Search Committee of the Department. He has authored/co-authored more than 200 research papers in peer reviewed international journals and conferences.

COURSE PLAN:

Week 1: L1: MOS Transistor Basic-I; L2: MOS Transistor Basic-I; L3: MOS Transistor Basic-II; L4: MOS Parasitic & SPICE Model; L5: CMOS Inverter Basics-I

Week 2: L1: CMOS Inverter Basics-II; L2: CMOS Inverter Basics-III; L3: Power Analysis-I; L4: Power Analysis-II; L5: SPICE Simulation-I

Week 3: L1: SPICE Simulation-II; L2: Combinational Logic Design-I; L3: Combinational Logic Design-II; L4: Combinational Logic Design-III; L5: Combinational Logic Design-IV

Week 4: L1: Combinational Logic Design-V; L2: Combinational Logic Design-VI; L3: Combinational Logic Design-VII; L4: Combinational Logic Design-VIII; L5: Combinational Logic Design-IX

Week 5: L1: Combinational Logic Design-X; L2: Logical Efforts-I; L3: Logical Efforts-II; L4: Logical Efforts-III; L5: Sequential Logic Design-I

Week 6: L1: Sequential Logic Design-II; L2: Sequential Logic Design-III; L3: Sequential Logic Design-IV; L4: Sequential Logic Design-V; L5: Sequential Logic Design-VI

Week 7: L1: Sequential Logic Design-VII; L2: Sequential Logic Design-VIII; L3: Clock Strategies for Sequential Design-I; L4: Clock Strategies for Sequential Design-II; L5: Clock Strategies for Sequential Design-III

Week 8: L1: Clock Strategies for Sequential Design-IV; L2: Sequential Logic Design-IX; L3: Clock Strategies for Sequential Design-V; L4: Concept of Memory & its Designing-I; L5: Concept of Memory & its Designing-II