ARCHITECTURAL DESIGN OF DIGITAL INTEGRATED CIRCUITS

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TYPE OF COURSE : Rerun | Elective | UG/PG
COURSE DURATION : 12 weeks (18 Jan' 21-09 Apr '21)
EXAM DATE : 24 April 2021

PRE-REQUISITES : Basic Digital Electronics Design
INTENDED AUDIENCE : Computer Science, Electrical Engineering, Electronics & Communication Engineering
INDUSTRIES APPLICABLE TO : Intel, Samsung, Freescale, Texas Instruments

COURSE OUTLINE :
Digital arithmetic plays an important role in the design of general-purpose digital processors and of embedded systems for signal processing, graphics, and communications. In spite of a mature body of knowledge in digital arithmetic, each new generation of processors or digital systems creates new arithmetic design problems. Designers, researchers, and graduate students will find solid solutions to these problems in this course. This course explains the fundamental principles of algorithms available for performing arithmetic operations on digital computers. These include basic arithmetic operations like addition, subtraction, multiplication, and division in fixed-point and floating-point number systems as well as more complex operations such as square root extraction and evaluation of exponential, logarithmic, and trigonometric functions. The algorithms described are independent of the particular technology employed for their implementation.

ABOUT INSTRUCTOR :
Indranil Hatai received his B.E. degree in Electronics and Communication Engineering from University of Burdwan, West Bengal, India and the M.S. (by research) and the Ph.D degree in Microelectronics and VLSI design from the department of Electronics and Electrical Communication Engineering, Indian Institute of Technology Kharagpur, India. Presently he is an Adjunct Professor in the Myanmar Institute of Information Technology, Mandalaya Myanmar. His research interest includes reconfigurable architecture of digital filters, FPGA based system design, software defined radio and VLSI based signal processing system design. He has served as a reviewer for IEEE Transactions on Circuits and System I: Regular Papers, IEEE Transactions on Signal Processing Letters, IEEE Transactions on Signal Processing, IEEE Transactions on very Large Scale Integration (VLSI) Systems and IEEE Transactions on Computer Aided Design for Integrated Circuits.

COURSE PLAN :

Week 1**:** Efficient technique/s for Algorithm to Architecture Mapping

Week 2**:** Efficient technique/s for Algorithm to Architecture Mapping (continued)

Week 3**:** Recent Trends on Adder/Subtractor Design

Week 4**:** Recent Trends on Multiplier/Divider Design(continued)

Week 5**:** Efficient VLSI Architectures for Various DSP blocks (FIR filter, CORDIC, FFT etc)

Week 6**:** Efficient VLSI Architectures for Various DSP blocks (continued)

Week 7**:** Fundamentals of Efficient Design and Implementation strategies of Digital VLSI Design (Clock Tree synthesis, Timing Closure, Synthesis

Week 8**:** Fundamentals of Efficient Design and Implementation strategies of Digital VLSI Design (continued)

Week 9 : Static Timing Analysis

Week 10 : Clock Skew

Week 11 : VLSI Interview FAQs

Week 12 **:** Tips and tricks for Digital VLSI based IC design