COURSE OUTLINE:
The course will introduce the participants to the Verilog hardware description language. It will help them to learn various digital circuit modeling issues using Verilog, writing test benches, and some case studies.

ABOUT INSTRUCTOR:
Prof. Indranil Sengupta has obtained his B.Tech., M.Tech. and Ph.D. degrees in Computer Science and Engineering (CSE) from the University of Calcutta. He joined the Indian Institute of Technology, Kharagpur, as a faculty member in 1988, in the Department of CSE, where he is presently a full Professor. He had been the former Heads of the Department of Computer Science and Engineering and also the School of Information Technology of the Institute. He has over 28 years of teaching and research experience. He has guided 22 PhD students, and has more than 200 publications to his credit in international journals and conferences.

COURSE PLAN:

Week 01: Introduction to digital circuit design flow (3 hours)
Week 02: Verilog variables, operators and language constructs (2 hours)
Week 03: Modeling combinational circuits using Verilog (2 hours)
Week 04: Modeling sequential circuits using Verilog (3 hours)
Week 05: Verilog test benches and design simulation (2 hours)
Week 06: Behavioral versus structural design modeling (2 hours)
Week 07: Miscellaneous modeling issues: pipelining, memory, etc. (2 hours)
Week 08: Processor design using Verilog (4 hours)