



C-BASED VLSI DESIGN

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Department of CSE
IIT Guwahati

TYPE OF COURSE : New | Elective | UG/PG

COURSE DURATION : 12 Weeks (26-Jul' 21 - 15-Oct' 21)

EXAM DATE : 24 Oct 2021

PRE-REQUISITES : Basic knowledge of digital design; Basic knowledge of Data structures and algorithms; Basic knowledge of Verilog. The students may go through the first six lectures of <https://nptel.ac.in/courses/106/105/106105083/> to learn Verilog.

INTENDED AUDIENCE : Final year BTech Student, MTech and PhD students, engineers from VLSI industries

INDUSTRIES APPLICABLE TO : Synopsys, Cadence, Mentor Graphics, Intel, Xilinx

COURSE OUTLINE :

This course discussed how a C code can be automatically translated into register transfer level (RTL) design using high-level synthesis (HLS). HLS is an active domain of research in recent times in the domain of electronic Design Automation (EDA) of VLSI. This course will help the student to (i) understand the overall HLS flow, (ii) how a C-code will be converted to its equivalent hardware, (iii) how to write c-code for efficient hardware generation and (iv) how the common software compiler optimization can help to improve the circuit performance. Also, advanced topics like HLS for FPGA targets, HLS for Security, optimizations at RTL level and verification challenges of HLS will be covered. This course will help the student to take up research in the domain of HLS. Also, this course will help the student to become proficient for EDA industries.

ABOUT INSTRUCTOR :

Dr. Chandan Karfa is an Assistant Professor in the Dept. of CSE, IIT Guwahati since 2016. He has over fifteen years of teaching and research experience. He has so far taught many courses in UG and PG level in IIT Guwahati. He has worked for five years as Senior R&D engineer in EDA Industry in the domain of High-level Synthesis and Logic Synthesis. He has worked as visiting researcher at New York University, May - July 2019. His research interests include High-level Synthesis, CAD for VLSI, Hardware Security and Formal Verification. He is an IEEE Senior member. He was recently awarded the Qualcomm Faculty Award 2021 which recognizes distinguished faculty research that inspires students and sparks new approaches in key technology areas.

COURSE PLAN :

Week 1: Introduction to Electronic Design Automation

Week 2: Introduction to C-based VLSI Design: Background

Week 3: Introduction to C-based VLSI Design: HLS Flow

Week 4: C-Based VLSI Design: Scheduling

Week 5: C-Based VLSI Design: Resource allocation and Binding, Data-path and Controller Generation

Week 6: Efficient Synthesis of C Code

Week 7: Hardware Efficient C Coding

Week 8: Impact of Compiler Optimizations in Hardware

Week 9: Verification of High-level Synthesis

Week 10: FPGA Technology Mapping

Week 11: Securing Design with High-level Synthesis

Week 12: Recent Advances in C-Based VLSI Design