PRE-REQUISITES : Computer Architecture (2nd year level)

INTENDED AUDIENCE : UG and PG students (Computer Science and Electrical Engineering)

INDUSTRIES APPLICABLE TO : Intel, AMD, IBM, Qualcomm, Texas Instruments

COURSE OUTLINE :
This course is on Advanced Computer Architecture. It will introduce students to advanced aspects of processor design and will specifically focus on out-of-order pipelines, GPUs, and compiler techniques for enhancing ILP. The course will subsequently move on to cache design and main memory technologies such as DDR-4. A substantial portion of the course will be devoted to the theory of on-chip networks and memory models. The last part of the course will cover aspects of low-power design, hardware security, and reliability.

ABOUT INSTRUCTOR :
Dr. Smruti R. Sarangi is an Associate Professor in the Computer Science and Engineering department at IIT Delhi. He has a Ph.D in computer science from the University of Illinois at Urbana Champaign, USA, and a B.Tech from IIT Kharagpur. Prior to his appointment as a faculty member in IIT Delhi in 2011, he spent 5 years working for IBM Research Labs, and Synopsys Research. He has published 60 papers in prestigious international conferences and journals, and holds 5 US patents. He is a member of the IEEE and ACM.

COURSE PLAN :
- **Week 1**: In-order pipelines overview
- **Week 2**: Out-of-order pipelines, Branch prediction
- **Week 3**: Advanced branch prediction techniques
- **Week 4**: Issue, select, and commit
- **Week 5**: Aggressive speculation
- **Week 6**: Compiler techniques for enhancing ILP
- **Week 7**: Caches: Design, modeling, and optimizations
- **Week 8**: On-chip networks
- **Week 9**: Theory of memory models
- **Week 10**: Coherence Protocols
- **Week 11**: Low power design
- **Week 12**: Reliability and Hardware Security