WEEK 1 ASSIGNMENT

The due date for submitting this assignment has passed. Due on 2016-07-31, 05:29 IST.

Submitted assignment

1) Determine the correct order of the design steps starting from initial concept to chip.  
   - Specification, Implementation, Prototyping, Manufacturing  
   - Specification, Prototyping, Implementation, Manufacturing  
   - Prototyping, Specification, Implementation, Manufacturing  
   - Manufacturing, Prototyping, Specification, Implementation

   No, the answer is incorrect.  
   Score: 0  
   Accepted Answers:  
   Specification, Implementation, Prototyping, Manufacturing

2) RTL (Register Transfer Logic) design is obtained as an output of __________ phase  
   - Architectural Synthesis  
   - Logic Synthesis  
   - Geometrical Synthesis  
   - High-Level Synthesis

   No, the answer is incorrect.  
   Score: 0  
   Accepted Answers:  
   Architectural Synthesis

3) __________ view describes the function of the circuit regardless of its implementation  
   - Physical  
   - Structural  
   - Behavioral  
   - Logic

   No, the answer is incorrect.  
   Score: 0  
   Accepted Answers:  
   Behavioral

4) The sequence of steps involved in architectural synthesis:  
   - Scheduling, Allocation, Identifying hardware resources, Binding, Controller generation  
   - Identifying hardware resources, Scheduling, Allocation, Binding, Controller generation
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- Identifying hardware resources, Allocation, Binding, Scheduling, Controller generation
- Identifying hardware resources, Allocation, Scheduling, Binding, Controller generation

No, the answer is incorrect.
Score: 0

Accepted Answers:
Identifying hardware resources, Scheduling, Allocation, Binding, Controller generation

5) Registers are connected to functional units via ______ and functional units are connected to registers via ______

- MUXs, DMUXs
- DMUXs, MUXs

No, the answer is incorrect.
Score: 0

Accepted Answers:
MUXs, DMUXs

6) Micro-architectural optimization happens in the ______ phase

- Architectural Synthesis
- Logic Synthesis
- Geometrical Synthesis
- High-level Synthesis

No, the answer is incorrect.
Score: 0

Accepted Answers:
Logic Synthesis

Registers are connected to functional units via ______ and functional units are connected to registers via ______

- MUXs, DMUXs
- DMUXs, MUXs

Micro-architectural optimization happens in the ______ phase

- Architectural Synthesis
- Logic Synthesis
- Geometrical Synthesis
- High-level Synthesis

No, the answer is incorrect.
Score: 0

Accepted Answers:
MUXs, DMUXs

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