Course outline

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Unit 5 - Week 3 :

Week 3 Assignment 3

The due date for submitting this assignment has passed.
As per our records you have not submitted this assignment.

1) Why is Flip Chip technology beneficial?
   - a. Availability of entire top surface for interconnections
   - b. Superior thermal management
   - c. Rugged construction compared to wire bonds
   - d. All of the above

   □ a.
   □ b.
   □ c.
   □ d.

   No, the answer is incorrect.
   Score: 0
   Accepted Answers:
   d.

2) Which company pioneered Flip Chip technology?
   - a. AT&T Bell Labs
   - b. Intel
   - c. International Business Machines
   - d. National Semiconductor

   □ a.
   □ b.
   □ c.
   □ d.
Why do we get superior signal integrity in Flip Chip packages?

a. Shorter electrical paths
b. Higher I/O count
c. Simultaneous connections in solder reflow
d. Better thermal management

No, the answer is incorrect.
Score: 0
Accepted Answers:

4) Which of the wire bonding methods does not require heating?

a. Thermocompression
b. Thermosonic
c. Ultrasonic
d. Wedge bonding with gold wire

No, the answer is incorrect.
Score: 0
Accepted Answers:

c.

5) Which of the options below describe the detachment process in Wedge Bonding?

a. Clamp is stationery
b. Wedge tool is stationery
c. None of the above
d. Both a and b

No, the answer is incorrect.
Score: 0
Accepted Answers:
d.
1) Why is UBM necessary?
   a. Protect the connection points from abuse
   b. Improve surface conductivity
   c. Facilitate good bonding with solder
   d. Reduce capacitance

   No, the answer is incorrect.
   Score: 0
   Accepted Answers:
   c.

2) Which process is used in UBM?
   a. Photo Lithography
   b. Etching
   c. Electroless plating
   d. All of the above

   No, the answer is incorrect.
   Score: 0
   Accepted Answers:
   c.

3) What is the function of an under fill in Flip chip?
   a. Epoxy bonding of die with substrate
   b. Minimize CTE mismatch between Si and substrate
   c. Improve I/O count
   d. Better electrical signal processing

   No, the answer is incorrect.
   Score: 0
   Accepted Answers:
   b.
Which of the following package designs help in reducing footprint?

a. PoP  
b. 3D die stacking  
c. MCM  
d. All of the above

No, the answer is incorrect.  
Score: 0  
Accepted Answers:  

Which of the above describes SoC?

a. Intense integration, low performance  
b. Increased functionality, low speed  
c. High performance, low power  
d. Complex fabrication, miniaturized form factor

No, the answer is incorrect.  
Score: 0  
Accepted Answers:  

c.  
d.