Week 6 Assessment

The due date for submitting this assignment has passed. As per our records you have not submitted this assignment.

1) Hard bake is done primarily between:
   - Lithography and development process
   - Development and etching
   - Spin coating and lithography
   - Deposition and spin coating
   Accepted Answer: Lithography and development process

2) Antenna is which zone to remove:
   - Gold
   - Nickel
   - Photolithography
   - Chromium
   Accepted Answer: Photolithography

3) Process of testing ELIs after you have monolith developer will have the sequence of:
   - Mask layout
   - Mask etching
   - Developing
   - Post bake
   Accepted Answer: Mask layout, Mask etching, Developing, Post bake

4) PECVD is an example of:
   - Plasma mechanical
   - Plasma electrostatic
   - Plasma elastomer
   - Plasma resistor
   Accepted Answer: Plasma mechanical

5) For Si L, photolithography is followed by:
   - Hard bake
   - Soft bake
   - Photo resist
   - Adhesive
   Accepted Answer: Hard bake

6) Arsenic doping is helpful in:
   - Hardening of Si surface
   - Softening of Si surface
   - Increasing conductivity
   - Decreasing conductivity
   Accepted Answer: Hardening of Si surface

7) Deposition techniques for depositing metal have excellent step coverage:
   - True
   - False
   Accepted Answer: False

8) SOI-4 pillars are used for:
   - Ensuring electrical contacts on IDEs
   - Transferring force onto piezoelectric material
   - Resistive
   - Conductive
   Accepted Answer: Ensuring electrical contacts on IDEs

9) SOI have a thin layer of silicon over a thick layer of silicon separated by a thin layer of insulator:
   - True
   - False
   Accepted Answer: False

10) Silicon nitride is grown over substrate for compensating stress in substrate due to Silicon oxide:
    - True
    - False
    Accepted Answer: True

You were allowed to submit this assignment only once.