Assignment 2

Due date for submitting this assignment has passed.
As per our records you have not submitted this assignment.

1) The overshoot in the transient response of the inverter due to: 1 point
   - Cip
   - Cet
   - Cip + Cet
   - Cet
   - No, the answer is incorrect.
   - Scale: 5
   - Accepted Answers: Cip

2) In the inverter chain, the optimal number of stages for minimum delay equals to: 1 point
   - N
   - N + 1
   - N - 1
   - No, the answer is incorrect.
   - Scale: 5
   - Accepted Answers: N

3) An optimum SDT must exist for the supply voltage: 1 point
   - 2.4 V
   - 3.0 V
   - 0.4 V
   - 2.0 V
   - No, the answer is incorrect.
   - Scale: 5
   - Accepted Answers: 1.8 V

4) Reduction in power dissipation can be brought by: 1 point
   - Increasing transistor area
   - Decreasing transistor area
   - Increasing transistor failure rate
   - Decreasing transistor failure rate
   - No, the answer is incorrect.
   - Scale: 5
   - Accepted Answers: Increasing transistor area

5) Calculate the power dissipation in a CMOS inverter. Consider a CMOS inverter with a load capacitance of $C_L = 2 \text{ pf}$ based at $VDD = 5 \text{ V}$. 'The inverter switches at a frequency of $f = 100 \text{ kHz}$. 1 point
   - $W = \frac{2}{3}VDD^2 C_L f$
   - $W = \frac{2}{3}VDD C_L f$
   - $W = \frac{2}{3}VDD^2 C_L f$
   - $W = \frac{2}{3}VDD C_L f$
   - No, the answer is incorrect.
   - Scale: 5
   - Accepted Answers: $W = \frac{2}{3}VDD^2 C_L f$

6) When the logic of the CMOS inverter is equal to input, the transistors are operating in: 1 point
   - N-MOS is cut-off, P-MOS is in Saturation
   - P-MOS is cut-off, N-MOS is in Saturation
   - Both the transistors are in active region
   - Both the transistors are in saturation region
   - No, the answer is incorrect.
   - Scale: 5
   - Accepted Answers: Both the transistors are in saturation region

7) We have a total of four toggles of the output over the duration of eight clock cycles. What is the activity factor? 1 point
   - 25%
   - 50%
   - 2525
   - 25
   - No, the answer is incorrect.
   - Scale: 5
   - Accepted Answers: 25%

8) Calculate the gain of a pseudo-NMOS inverter at the threshold voltage without ignoring the transistor output impedances. Assume $V_{DD}=3 \text{ V}$. 1 point
   - $-\frac{1}{2}$
   - $-\frac{1}{3}$
   - $-\frac{1}{4}$
   - $-\frac{1}{10}$
   - No, the answer is incorrect.
   - Scale: 5
   - Accepted Answers: $-\frac{1}{2}$

9) Statement: The instant deep of the inverter (ip) is independent of the sizing of the gate. Statement is true: 1 point
   - True
   - False
   - $VDD$ is constant due to MOS transistor
   - Both false
   - No, the answer is incorrect.
   - Scale: 5
   - Accepted Answers: False

10) When Kirchhoff, threshold voltage moves closer to: 1 point
    - zero
    - utopia
    - midpoint voltage
    - Supply voltage
    - No, the answer is incorrect.
    - Scale: 5
    - Accepted Answers: zero