Unit 10 - Week 8

Assignment 8

The due date for submitting this assignment has passed.
As per our records you have not submitted this assignment.

Due on 2020-03-25, 23:59 IST.

1) State whether the following statement is true or false. "Valley current-mode control offers a better line transient response compared to peak current-mode control." *1 point*

- True
- False

No, the answer is incorrect.
Score: 0
Accepted Answers:
False

2) Which of the following statements is true (ignoring all losses) for a current-mode DC-DC converter with V_{in} = 2.5 V and V_{out} = 1.2 V? *1 point*

- Peak current-mode control is most suitable
- Valley current-mode control is most suitable
- Both peak and valley current-mode control are suitable
- Current mode control cannot be used

No, the answer is incorrect.
Score: 0
Accepted Answers:
Peak current-mode control is most suitable

3) State whether the following statement is true or false. "Operating a switching DC-DC converter in DCM is more power-efficient than operating it in CCM, for light loads." *1 point*

- True
- Flase

No, the answer is incorrect.
Score: 0
Accepted Answers:
True

Consider the gate driver buffers shown in Figure 1, for questions 4 to 7. Assume that the transistors in the gate driver buffers operate in the linear/triode region. All of the gate driver circuitry operates from a common supply voltage of 1.8 V. Adhere to the units mentioned in the question while filling in numerical answers. Use information provided / obtained in a previous question to answer subsequent questions.

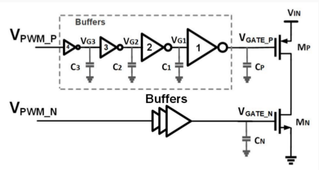

Figure 1

4) Fill in the blank with a numerical answer: Given C_P = 20 pF, the R_{DS_ON} of the PMOS and NMOS transistors used in inverter-1, that gives equal rise and fall times respectively (10% to 90% of V_{DD} and vice versa) of 100 ps, is ____ Ω (up to 2 decimal places). *1 point*

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Range) 2,2.5

5) Fill in the blank with a numerical answer: Given $\mu_p C_{ox}$ = 50 μA/V^2 and $|V_{Tp}|$ = 0.5 V, the W/L ratio of the PMOS transistor used in inverter-1, that is required to achieve a rise time (10% to 90% of V_{DD}) of 100 ps, is ____ x 10^3 (up to 2 decimal places). *1 point*

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Range) 6.15,7.7

6) Fill in the blank with a numerical answer: Given $\mu_n C_{ox}$ = 150 μA/V^2 and V_{Tn} = 0.5 V, the W/L ratio of the NMOS transistor used in inverter-1, that is required to achieve a fall time (90% to 10% of V_{DD}) of 100 ps, is ____ x 10^3 (up to 2 decimal places). *1 point*

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Range) 2,2.6

7) Fill in the blank with a numerical answer: The ratio of the load capacitance at the output of an inverter to its input capacitance is defined as the fanout of the inverter. Assuming, (i) that the fanout scales linearly with the W/L ratio of the inverter's transistors, and (ii) that every inverter has a fanout of 10, the W/L ratio of the PMOS transistor used in inverter-4, that gives equal rise times (10% to 90% of V_{DD}) of 100 ps at the output of every inverter, is ____ (up to 2 decimal places). *1 point*

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Range) 6.15,7.7

8) Consider the ramp generator circuit shown in Figure 2, for question 8. Adhere to the units mentioned in the question while filling in numerical answers. *1 point*

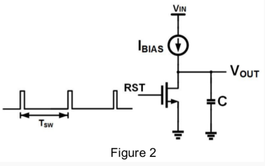

Figure 2

Fill in the blank with a numerical answer: Given that I_{BIAS} = 5 μA and assuming that the NMOS reset switch resets V_{OUT} instantaneously, the capacitance of the capacitor C that is required to generate a ramp for trailing-edge PW modulation at F_{SW} = 1 MHz, with a peak voltage V_{in} = 1 V, is ____ pF (no decimal places).

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Range) 4.99,5

Consider the zero-cross comparator shown in Figure 3, for questions 9 to 13. Adhere to the units mentioned in the question while filling in numerical answers. Use information provided / obtained in a previous question to answer subsequent questions.

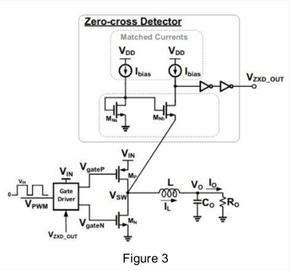

Figure 3

9) Fill in the blank with a numerical answer: Given that transistors M_{N1} and M_{N2} operate in the saturation region, $\mu_n C_{ox}$ = 150 μA/V^2, V_{Tn} = 0.5 V, I_{BIAS} = 1.5 μA and $(W/L)_{MN\_N4} = (W/L)_{MN\_N3}$ = 2 (when transistors M_{N1} and M_{N2} are perfectly matched), then ignoring the effect of channel length modulation, the gate-to-source voltage V_{GS} of transistor M_{N2} , at which the zero-crossing of the switching node V_{SW} is detected, is ____ mV (no decimal places). *1 point*

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 600

10) Fill in the blank with a numerical answer (include the sign as well): Supposing that transistor M_{N1} is not perfectly matched with transistor M_{N2} , in that M_{N1} has a current factor that is greater than that of M_{N2} by 5% (while M_{N2} has the value mentioned in question 9), the zero-crossing of the switching node V_{SW} is detected with an offset of ____ mV (up to 1 decimal place). *1 point*

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Range) 2.2,2.6

11) Fill in the blank with a numerical answer (include the sign as well): Given V_{IN} = 1.8 V, V_O = 1 V, L = 1 μH, switching frequency (F_{SW}) = 5 MHz and $R_{DS\_ON\_MP} = R_{DS\_ON\_MN}$ = 100 mΩ, the value of the inductor current at which the zero-crossing of the switching node V_{SW} is detected (in respect of question 10) is ____ mA (up to 1 decimal place). *1 point*

Additional exercise (not evaluated): Find the duration over which M_N remains ON, during T_{OFF} , in terms of the load current.
Hint: Use the expression for the voltage conversion ratio in DCM.

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Range) -26,-22

12) Fill in the blank with a numerical answer (include the sign as well): Supposing that transistor M_{N1} is not perfectly matched with transistor M_{N2} , in that M_{N1} has a threshold voltage that is greater than that of M_{N2} by 2% (while M_{N2} has the value mentioned in question 9), the zero-crossing of the switching node V_{SW} is detected with an offset of ____ mV (up to 1 decimal place). *1 point*

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Range) -11,-9

13) Fill in the blank with a numerical answer (include the sign as well): Given V_{IN} = 1.8 V, V_O = 1 V, L = 1 μH, switching frequency (F_{SW}) = 5 MHz and $R_{DS\_ON\_MP} = R_{DS\_ON\_MN}$ = 100 mΩ, the value of the inductor current at which the zero-crossing of the switching node V_{SW} is detected (in respect of question 12) is ____ mA (up to 1 decimal place). *1 point*

Additional exercise (not evaluated): Find the duration over which M_N remains ON, during T_{OFF} , in terms of the load current.
Hint: Use the expression for the voltage conversion ratio in DCM.

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Range) 90,110

14) Fill in the blank with a numerical answer (specify only the absolute value): The inductor current in a peak-current-mode controlled switching converter rises (during T_{ON}) with a slope of 800 kA/s and falls (during T_{OFF}) with a slope of -1000 kA/s. The minimum possible slope of the compensating ramp that will stabilise the current loop of the converter is ____ kA/s (no decimal places). *1 point*

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 100