

Unit 8 - Week 6

Course outline

How does an NPTEL online course work?

Week 0

Week 1

Week 2

Week 3

Week 4

Week 5

Week 6

- Dominant Pole Compensation (Type-I with Gm-C Architecture)
- Dominant Pole Compensation (Type-I with Op Amp-RC Architecture)
- Introduction to Type-II Compensation
- Type-II Compensator using Gm-C Architecture - Part 1
- Type-II Compensator using Gm-C Architecture - Part 2
- Type-II Compensator using Gm-C Architecture - Part 3
- Type-II Compensator using Op Amp-RC Architecture
- Introduction to Type-III Compensator
- Type-III Compensator using Op Amp-RC Architecture
- Simulation of DC-DC Converter with Type-III Compensator
- Quiz : Assignment 6
- Week 6 Feedback

Week 7

Week 8

Week 9

Week 10

Week 11

Week 12

Download Videos

Assignment solutions

Assignment 6

The due date for submitting this assignment has passed. **Due on 2020-03-11, 23:59 IST.**
 As per our records you have not submitted this assignment.

Consider the circuit shown in Figure 1, for questions 1 to 10. The cascade of a type-I compensated buck converter with an LDO is designed for the following specifications. $V_{IN} = 1.8\text{ V}$, $V_O = 1.0\text{ V}$, $V_{DROP} = 200\text{ mV}$, switching frequency (F_{SW}) = 5 MHz, $L = 1\text{ }\mu\text{H}$, $C_X = C_O = 4\text{ }\mu\text{F}$, $R_O = 1\text{ }\Omega$, $g_m = 100\text{ }\mu\text{S}$. Assume that inductor $R_{DCR} = 50\text{ m}\Omega$, R_{DS_ON} of M_p is 50 m Ω , forward voltage of diode D_N is 300 mV and peak-to-peak amplitude of V_{RAMP} is 0.5 V.

Adhere to the units mentioned in the question while filling in numerical answers. The duty cycle D always lies between 0 and 1.

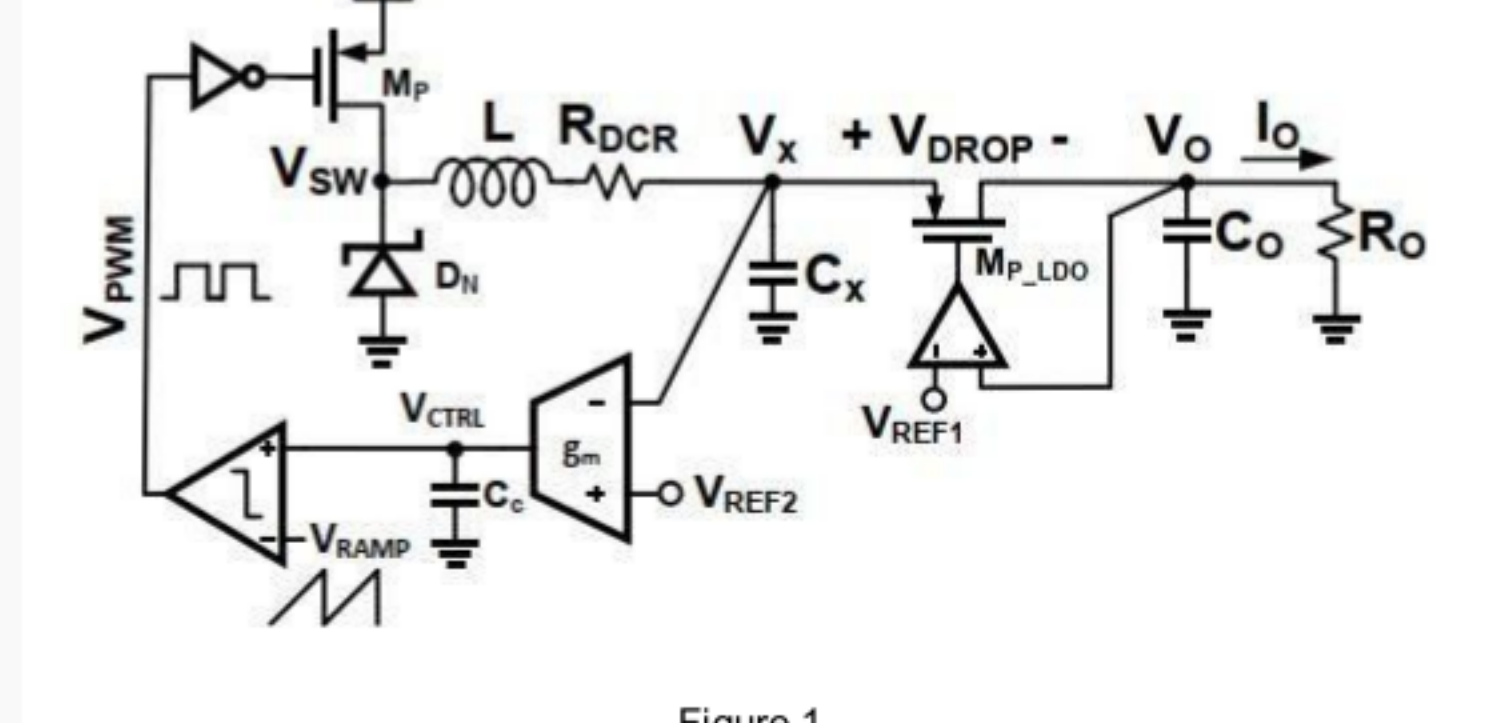


Figure 1

1) Fill in the blank with a numerical answer: The duty cycle of V_{PWM} (in respect of the circuit shown in Figure 1) is $D = \underline{\hspace{2cm}}$ (up to 2 decimal places).

No, the answer is incorrect.
 Score: 0
 Accepted Answers: (Type: Range) 0.72,0.8

2 points

2) Fill in the blank with a numerical answer: The control voltage V_{CTRL} (in respect of the circuit shown in Figure 1) corresponding to the duty cycle of V_{PWM} found in question 1 is $\underline{\hspace{2cm}}$ volt (up to 2 decimal places).

No, the answer is incorrect.
 Score: 0
 Accepted Answers: (Type: Range) 0.35,0.4

1 point

3) Fill in the blank with a numerical answer: The peak-to-peak inductor ripple current ΔI_L (in respect of the circuit shown in Figure 1) is $\underline{\hspace{2cm}}$ mA (up to 1 decimal place).

No, the answer is incorrect.
 Score: 0
 Accepted Answers: (Type: Range) 72,92

1 point

4) Fill in the blank with a numerical answer: The average current (in respect of the circuit shown in Figure 1) drawn from the supply V_{IN} is $\underline{\hspace{2cm}}$ mA (up to 1 decimal place).

No, the answer is incorrect.
 Score: 0
 Accepted Answers: (Type: Range) 700,800

1 point

5) Fill in the blank with a numerical answer: The overall conduction efficiency of the system shown in Figure 1, ignoring losses due to the inductor ripple current is $\eta = \underline{\hspace{2cm}}$ % (up to 1 decimal place).

No, the answer is incorrect.
 Score: 0
 Accepted Answers: (Type: Range) 72,75

1 point

6) Fill in the blank with a numerical answer: Assuming that the ON resistance of diode D_N is 0 Ω , the quality factor of the inductor (in respect of the circuit shown in Figure 1) is $Q = \underline{\hspace{2cm}}$ (up to 1 decimal place).

No, the answer is incorrect.
 Score: 0
 Accepted Answers: (Type: Range) 1.3,6

1 point

7) Fill in the blank with a numerical answer: Assuming that the ON resistance of diode D_N is 0 Ω , the minimum value of the compensation capacitor C_C (in respect of the circuit shown in Figure 1) for which the loop is stable with a gain margin of -6 dB under no-load condition is $\underline{\hspace{2cm}}$ nF (up to 1 decimal place).

No, the answer is incorrect.
 Score: 0
 Accepted Answers: (Type: Range) 7.8,10

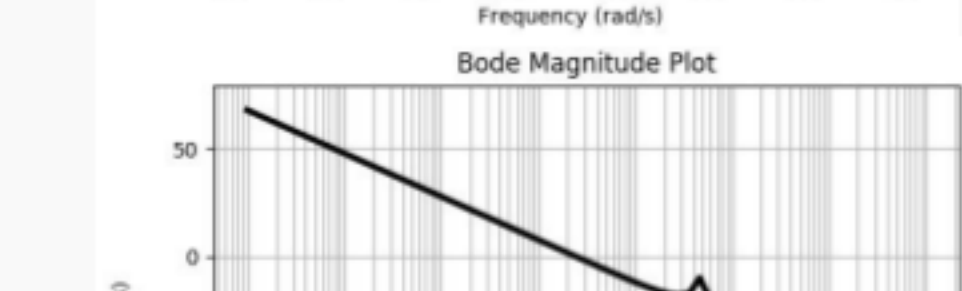
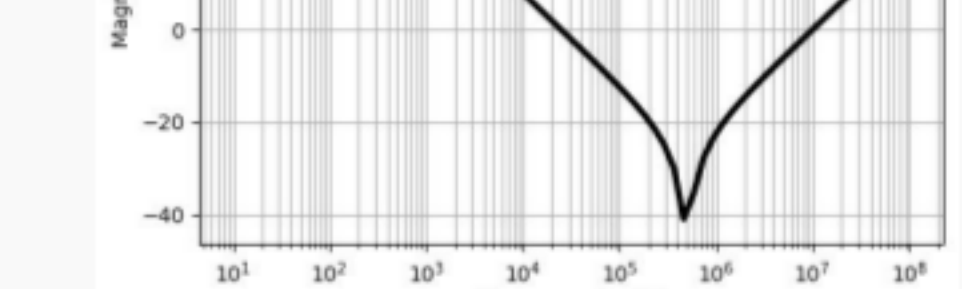
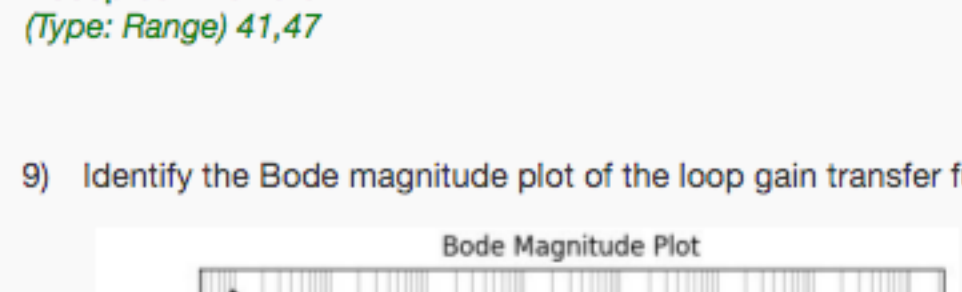
2 points

8) Fill in the blank with a numerical answer: The unity loop gain frequency of the system shown in Figure 1 is $\omega_{UGB} = \underline{\hspace{2cm}}$ krad/s (up to 1 decimal place).

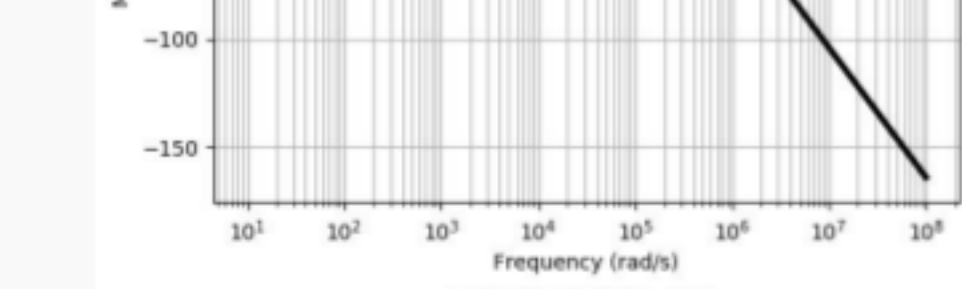
No, the answer is incorrect.
 Score: 0
 Accepted Answers: (Type: Range) 41,47

1 point

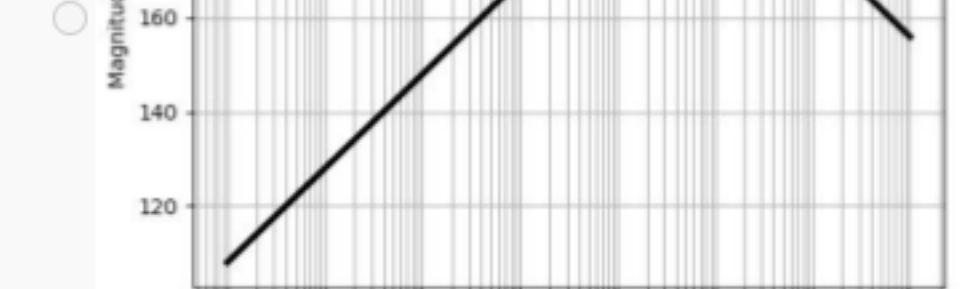
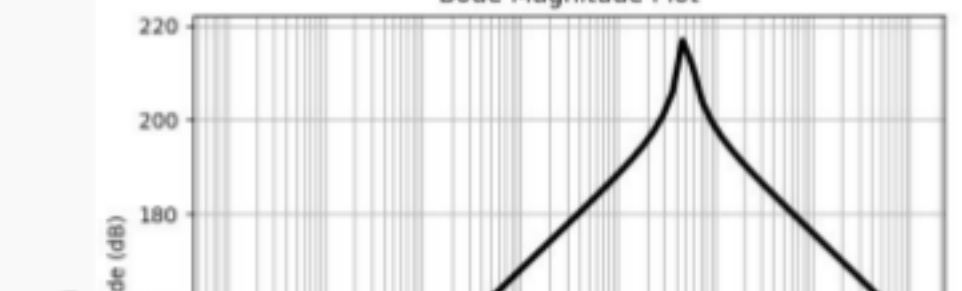
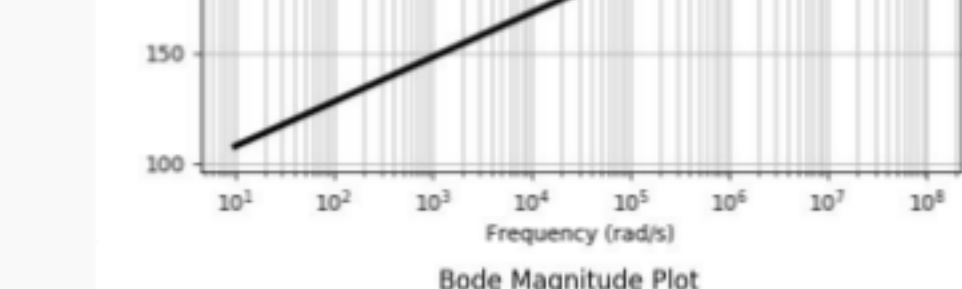
9) Identify the Bode magnitude plot of the loop gain transfer function (in respect of the circuit shown in Figure 1) amongst the choices provided below. **1 point**



No, the answer is incorrect.
 Score: 0
 Accepted Answers:



10) Identify the Bode phase plot of the loop gain transfer function (in respect of the circuit shown in Figure 1) amongst the choices provided below. **1 point**



No, the answer is incorrect.
 Score: 0
 Accepted Answers:

