Unit 5 - Week 3

Course outline

How does an NPTEL online course work?

Week 0

Week 1

Week 2

Week 3

- Dominant Pole Compensation using Miller Effect, RHP zero due to Miller Capacitor
- Intuitive Method of Finding the Poles, Pole Splitting after Miller Compensation
- Effect of RHP zero on Stability, Mitigating the Effect of RHP zero, LDO with NMOS Pass Element
- Output Impedance of PMOS LDO
- Line Regulation and PSRR of PMOS LDO
- PSRR of PMOS versus PSRR of NMOS LDO
- Sources of Error in Linear and Switching Regulators
- Offset in Amplifiers; Real Life Analogy; Static Offset Cancellation
- Dynamic Offset Cancellation Techniques (Chopping, Auto-zeroing)
- Quiz : Assignment 3
- Week 3 Feedback

Week 4

Week 5

Week 6

Week 7

Week 8

Week 9

Week 10

Week 11

Week 12

Download Videos

Assignment solutions

Assignment 3

The due date for submitting this assignment has passed.
As per our records you have not submitted this assignment.

Due on 2020-02-19, 23:59 IST.

1) Which pass element is more suitable for low-voltage operation of an LDO and why? *1 point*

- NMOS pass transistor because it has higher mobility of charge carriers
- PMOS pass transistor because it has lower mobility of charge carriers
- NMOS pass transistor because it doesn't require additional charge pumps
- PMOS pass transistor because the gate voltage is always lower than the input voltage

No, the answer is incorrect.
Score: 0
Accepted Answers:
PMOS pass transistor because the gate voltage is always lower than the input voltage

2) State whether the following statement is true or false. "The line regulation of an LDO can be improved by increasing the DC loop gain." *1 point*

- True
- False

No, the answer is incorrect.
Score: 0
Accepted Answers:
False

3) Which of the following LDO topologies has the maximum power supply rejection ratio (PSRR)? *0 points*

- NMOS pass transistor and error amplifier with n-input differential pair
- PMOS pass transistor and error amplifier with p-input differential pair
- NMOS pass transistor and error amplifier with p-input differential pair
- PMOS pass transistor and error amplifier with n-input differential pair

No, the answer is incorrect.
Score: 0
Accepted Answers:
NMOS pass transistor and error amplifier with p-input differential pair

4) Which of the following statements are true for an LDO? *0 points*

- For a high PSRR, the dominant pole should be at the output of the LDO.
- For a high PSRR, the dominant pole should be at the gate of the pass transistor.
- Line regulation can be improved by increasing the bandwidth.
- Load regulation can be improved by increasing the loop gain.

No, the answer is incorrect.
Score: 0
Accepted Answers:
For a high PSRR, the dominant pole should be at the output of the LDO.
Load regulation can be improved by increasing the loop gain.

5) State whether the following statement is true or false. "The DC PSRR of an LDO can be improved by increasing the gain of the output stage." *1 point*

- True
- False

No, the answer is incorrect.
Score: 0
Accepted Answers:
False

6) Which of the following LDO topologies has the best power supply rejection ratio (PSRR)? *1 point*

- PMOS pass transistor with dominant pole at error amplifier output
- NMOS pass transistor with dominant pole at LDO output
- NMOS pass transistor with dominant pole at error amplifier output
- PMOS pass transistor with dominant pole at LDO output

No, the answer is incorrect.
Score: 0
Accepted Answers:
NMOS pass transistor with dominant pole at LDO output

7) If the output of an LDO is adjusted through the feedback resistors, which of the following statements is correct when it is operated at V_{IN} = 1.8 V, I_{LOAD} = 0 to 10 mA? *1 point*

- Load regulation is better at V_{OUT} = 1.2 V
- Load regulation is better at V_{OUT} = 1.5 V
- Load regulation is not affected when the output voltage is changed

No, the answer is incorrect.
Score: 0
Accepted Answers:
Load regulation is better at V_{OUT} = 1.2 V

Consider the small-signal picture of a common source amplifier as shown in Figure 1, for questions 8 and 9. Ignore all the intrinsic capacitances of M_P except C_{gs} and C_{gd} . Assume that the channel length modulation factor is $\lambda = 1\ V^{-1}$, R_D = 100 kΩ, C_{gs} = 250 fF, C_{gd} = 50 fF, quiescent I_D = 10 μA and gate overdrive voltage V_{ov} = 100 mV. Adhere to the units mentioned in the question while filling in numerical answers.

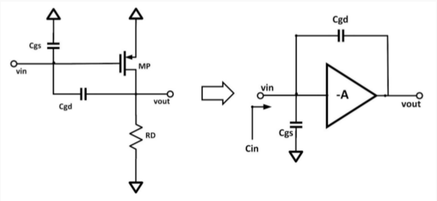

Figure 1

8) Fill in the blank with a numerical answer: The gain A of the common-source amplifier (in respect of the circuit shown in Figure 1) is ____ V/V (up to 1 decimal place). *2 points*

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 10

9) Fill in the blank with a numerical answer: The total capacitance seen at the input (gate) of the common-source amplifier (in respect of the circuit shown in Figure 1) is C_{in} = ____ fF (up to 1 decimal place). *2 points*

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Range) 720,880

Consider the circuit shown in Figure 2 for questions 10 to 12. The LDO is designed for V_{DD} = 1.6 V and V_O = 1.5 V with load current I_{LOAD} = 1 mA. Assume that the pass transistor M_P is in saturation with V_{OV} = 100 mV and that the channel length modulation factor is $\lambda = 1\ V^{-1}$. Adhere to the units mentioned in the question while filling in numerical answers.

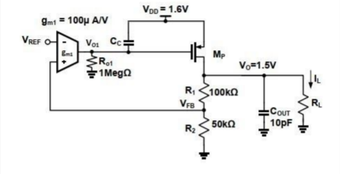

Figure 2

10) Fill in the blank with a numerical answer: The line regulation of the LDO (shown in Figure 2) is ____ mV/V (up to 1 decimal place). *1 point*

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Range) 28.5,31.5

11) Fill in the blank with a numerical answer: The DC loop gain of the LDO (shown in Figure 2) is ____ dB (up to 2 decimal places). *1 point*

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Range) 46.91,57.34

12) Fill in the blank with a numerical answer: The load regulation of the LDO (shown in Figure 2) is ____ Ω (up to 2 decimal places). *1 point*

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Range) 1.33,1.63