Unit 4 - Week 2

Assignment 2

The due date for submitting this assignment has passed.
As per our records you have not submitted this assignment.

Due on 2020-02-12, 23:59 IST.

1) State whether the following statement is true or false. "When an LDO is used as a sub-regulator in cascade with a switching regulator for stepping down the input voltage, it is more efficient to design the switching regulator to have the smaller step-down ratio of the two." *1 point*

True
False

No, the answer is incorrect.
Score: 0
Accepted Answers:
False

2) State whether the following statement is true or false. "When an LDO is used as an auxiliary current source in parallel with a switching regulator to improve the transient response, it should have a larger bandwidth than the switching regulator." *1 point*

True
False

No, the answer is incorrect.
Score: 0
Accepted Answers:
True

3) State whether the following statement is true or false. "The feedback loop in an LDO regulates the output voltage by changing the current through the pass element." *1 point*

True
False

No, the answer is incorrect.
Score: 0
Accepted Answers:
True

4) State whether the following statement is true or false. "Voltage regulation in an LDO is achieved by means of a positive feedback loop" *1 point*

True
False

No, the answer is incorrect.
Score: 0
Accepted Answers:
False

5) State whether the following statement is true or false. "Loop gain analysis in a feedback system applies to large-signal perturbations." *1 point*

True
False

No, the answer is incorrect.
Score: 0
Accepted Answers:
False

6) State whether the following statement is true or false. "Dominant pole compensation increases the unity-loop-gain bandwidth of a feedback system." *1 point*

True
False

No, the answer is incorrect.
Score: 0
Accepted Answers:
False

Consider the circuit shown in Figure 1 for questions 7 to 12. The LDO needs to be designed for V_{DD} = 1.6 V and V_O = 1.5 V with load current I_L varying from 0 to 1 mA. Ignore all the intrinsic capacitances of the pass transistor M_P . Assume that the channel length modulation factor, λ_P = 1 V^{-1} , $\mu_p C_{ox}$ = 50 $\mu A/V^2$ and $|V_{TH}|$ = 500 mV. Adhere to the units mentioned in the question while filling in numerical answers.

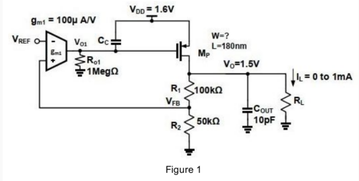


Figure 1

7) Fill in the blank with a numerical answer: The value of V_{REF} (in respect of the circuit shown in Figure 1) is ____ volt (up to 1 decimal place). *1 point*

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 0.5

8) Fill in the blank with a numerical answer: The minimum channel width W (in respect of the circuit shown in Figure 1) that is required to keep M_P in saturation for the entire load range of 0 to 1 mA is ____ µm (up to 1 decimal place). *2 points*

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Range) 654.5,800

9) Fill in the blank with a numerical answer: Assume that the dominant pole is at V_{O1} , the gate of the pass transistor M_P (in respect of the circuit shown in Figure 1) and that the width W of M_P is the minimum value calculated in question 8. Then, the value of the compensation capacitor C_C that is required to achieve a minimum phase margin of 60 degrees for the entire load range of 0 to 1 mA is ____ nF (up to 2 decimal places). *2 points*

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Range) 3.74,4.58

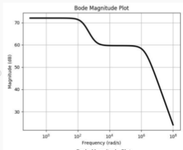
10) Fill in the blank with a numerical answer: The dominant pole (in respect of the circuit shown in Figure 1) at the gate of the pass transistor M_P , computed using the value of the compensation capacitor C_C obtained in question 9, lies at a frequency of ____ rad/s (up to 1 decimal place). *1 point*

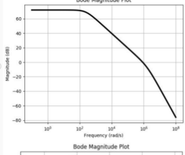
No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Range) 216.4,264.5

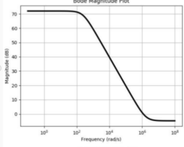
11) Fill in the blank with a numerical answer: The unity loop gain bandwidth (in respect of the circuit shown in Figure 1) computed using the value of the compensation capacitor C_C obtained in question 9, when the phase margin is the worst (i.e. 60 degrees) is ω_{UGB} = ____ krad/s (up to 1 decimal place). *1 point*

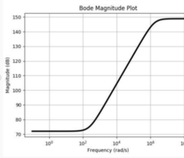
No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Range) 865.9,1058.4

12) Identify the Bode magnitude plot of the loop gain transfer function (in respect of the circuit shown in Figure 1) amongst the choices provided below. *1 point*









No, the answer is incorrect.
Score: 0
Accepted Answers: