Unit 13 - Week 11

Assignment 11

The due date for submitting this assignment has passed.
As per our records you have not submitted this assignment.

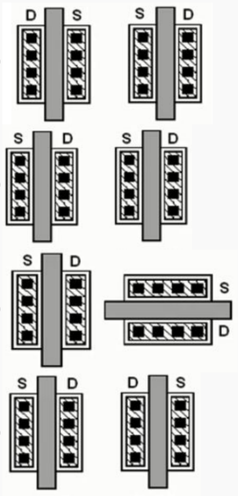
Due on 2020-04-15, 23:59 IST.

1) With respect to the avoidance of systematic mismatch through layout techniques, which of the following increase(s) the chance of device mismatch? *1 point*

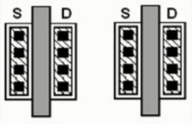
- Same device orientation
- Using common centroid method
- Small device sizes
- Using Dummy devices at boundary
- Placing devices far away

No, the answer is incorrect.
Score: 0
Accepted Answers:
Small device sizes
Placing devices far away

2) Identify the device placement configuration that ensures better matching between the two devices, amongst the choices provided below. *1 point*



No, the answer is incorrect.
Score: 0
Accepted Answers:



3) State whether the following statement is true or false. "Usage of guard rings during layout helps to suppress substrate noise." *1 point*

- True
- False

No, the answer is incorrect.
Score: 0
Accepted Answers:
True

Consider the digitally-controlled DC-DC converter shown in Figure 1, for questions 4 to 7. Assume that V_{in} = 1.8 V and that V_{out} = 0.8 V. Ignore all losses & delays. Use information provided / obtained in a previous question to answer subsequent questions. Adhere to the units mentioned in the question while filling in numerical answers. The duty cycle D always lies between 0 and 1.

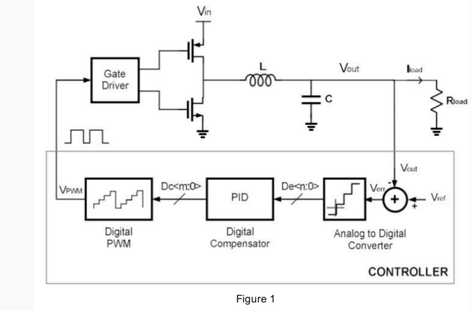


Figure 1

4) Fill in the blank with a numerical answer: Assume that the overshoot/undershoot of V_{out} is always within ± 400 mV and that the ADC is linear. If the DC regulation specification is 0.5% of V_{out} , then the ADC needs to have a minimum resolution of n = ____ bits (no decimal places).

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 8

1 point

5) Fill in the blank with a numerical answer: If the overshoot/undershoot of V_{out} is not expected to exceed ± 50 mV, then assuming uniform quantization, the minimum resolution of the ADC that can be used to satisfy the DC regulation specification mentioned in question 4, is n = ____ bits (no decimal places).

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 5

1 point

6) Fill in the blank with a numerical answer: The maximum step size of the DPWM duty cycle, that can achieve the DC regulation specification mentioned in question 4, is ____ x 10^{-3} (up to 2 decimal places).

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Range) 2,2.22

1 point

7) State whether the following statement is true or false. "To avoid limit cycle oscillations, the resolution of the DPWM should be smaller than the resolution of the ADC." *1 point*

- True
- False

No, the answer is incorrect.
Score: 0
Accepted Answers:
False

8) State whether the following statement is true or false. "Middlebrooke's method of measuring the gain-crossover frequency and phase margin of a feedback loop involves breaking the loop and injecting a variable-frequency square wave signal." *1 point*

- True
- False

No, the answer is incorrect.
Score: 0
Accepted Answers:
False

9) Which of these provides proportional gain in a time-based PID controller? *1 point*

- Voltage-Controlled Oscillator (VCO)
- Voltage-Controlled Delay Line (VCDL)
- Phase Detector (PD)
- Phase Frequency Detector (PFD)

No, the answer is incorrect.
Score: 0
Accepted Answers:
Voltage-Controlled Delay Line (VCDL)

10) Which of these benefits accrue by dynamically varying the supply voltage and clock frequency (DVFS) of digital circuitry? *1 point*

- Conservation of power when data rate is low
- Prevention of system overheating and thermal runaway
- Increase in lifespan of undervolted devices by avoiding hot carrier injection and electromigration
- All of the above

No, the answer is incorrect.
Score: 0
Accepted Answers:
All of the above