

Unit 10 - Week 8 - pMOS transistor; Converting pMOS circuits to nMOS

Course outline

How does an NPTEL online course work?

Week 0

Week 1 - Obtaining power gain and need for nonlinearity

Week 2 - Nonlinear two ports; MOS transistor; Common source amplifier

Week 3 - Common source amplifier using the MOS transistor

Week 4 - Biasing a MOS transistor at a fixed drain current; CS amplifier using drain feedback bias and current mirror bias

Week 5 - CS amplifier using source feedback bias; Controlled sources using a MOS transistor-VCVS

Week 6 - Controlled sources continued-VCCS, CCCS, CCVS

Week 7 - Opamp controlled sources; Virtual short; Swing limits; Summary of amplifiers

Week 8 - pMOS transistor; Converting pMOS circuits to nMOS

- pMOS transistor
- Small signal model of the pMOS transistor
- Common source amplifier using the pMOS transistor
- Swing limits of the pMOS common source amplifier
- Biasing a pMOS transistor at a constant current; pMOS current mirror
- Converting nMOS transistor circuits to pMOS
- Bias current generation
- Examples of more than one transistor in feedback
- Quiz : Assignment 8
- Analog Circuits: Week 8 Feedback form
- Assignment 8 Solutions

Week 9 - Common source amplifier with active load; CMOS inverter

Week 10 - Differential pair with current mirror load; Single-stage opamp

Week 11 - Two-stage opamp; Opamp characteristics

Week 12 - Bipolar transistors

Lecture Notes

Text Transcripts

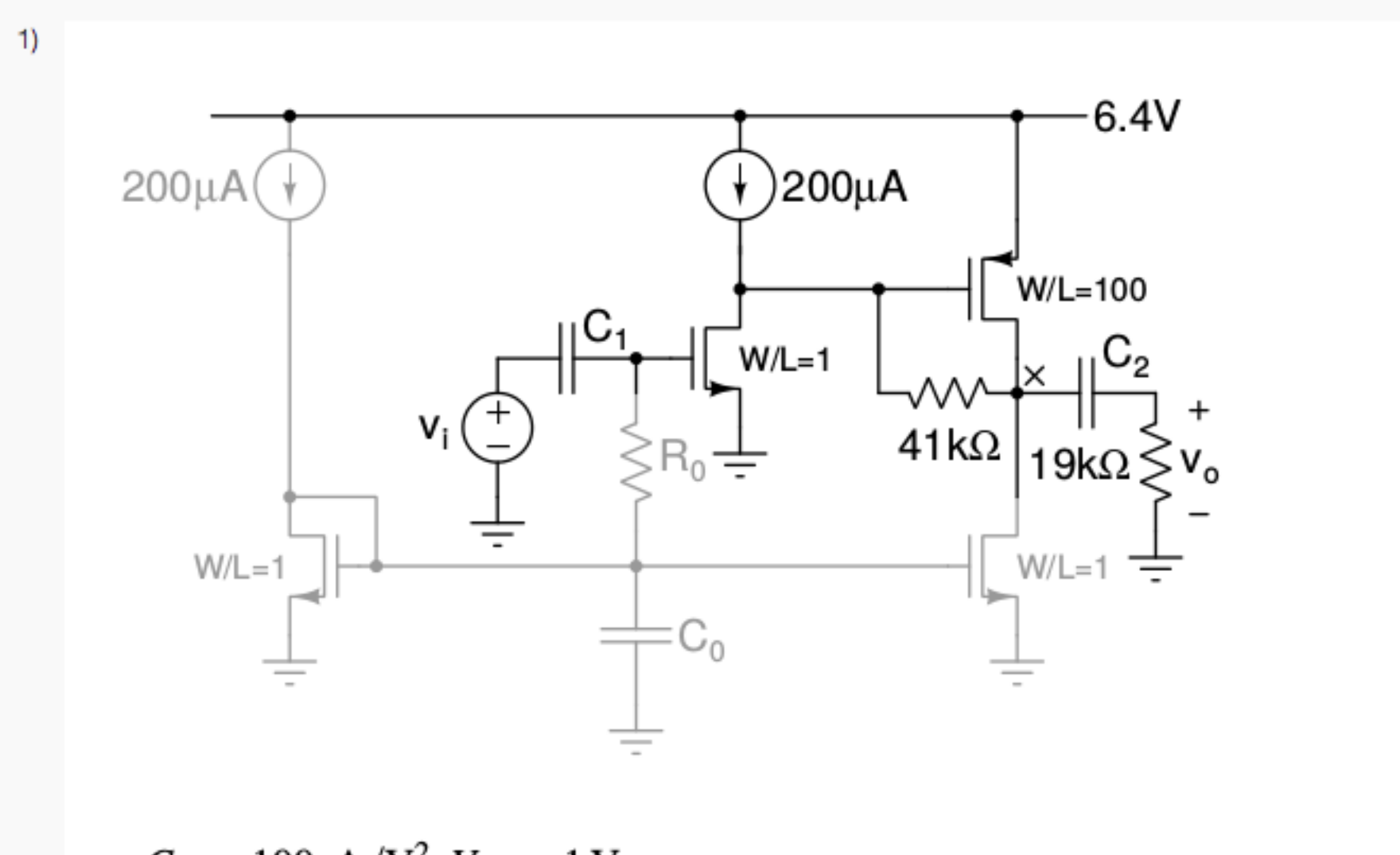
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Assignment 8

The due date for submitting this assignment has passed. As per our records you have not submitted this assignment.

Due on 2020-03-25, 23:59 IST.



$\mu_n C_{ox} = 100\mu\text{A}/\text{V}^2$, $V_{Tn} = 1\text{ V}$.
 $\mu_p C_{ox} = 25\mu\text{A}/\text{V}^2$, $V_{Tp} = 1\text{ V}$.
 W/L ratios are shown next to respective transistors.
 $C_{0,1,2}$ and R_G are very large.

(Don't panic at the number of transistors! First try to ascertain the function of each transistor. For your convenience, biasing parts are shown in gray. For example, if you figure out that small signal v_{GS} is zero for some transistor, you don't have to include its controlled source in the small signal analysis.)

Determine the voltage at node x at the operating point.

(The answer must be in volts (V). Round off fractional answers to one decimal place.)

No, the answer is incorrect.
 Score: 0
 Accepted Answers:
 (Type: Numeric) 5

1 point

2) Determine the gain v_o/v_i . Assume that all capacitors are large.

(The answer must be the value of the gain. Round off fractional answers to one decimal place.)

No, the answer is incorrect.
 Score: 0
 Accepted Answers:
 (Type: Range) 7.4,7.6

1 point

3) Determine the maximum positive value of v_i for which all transistors remain in the desired region, i.e. neither in triode region nor cutoff (For this, you have to calculate the limit on v_i induced by each transistor entering triode region or cutoff and take the worst case).

(The answer must be in volts (V). Round off fractional answers to two decimal places.)

No, the answer is incorrect.
 Score: 0
 Accepted Answers:
 (Type: Range) 0.12,0.13

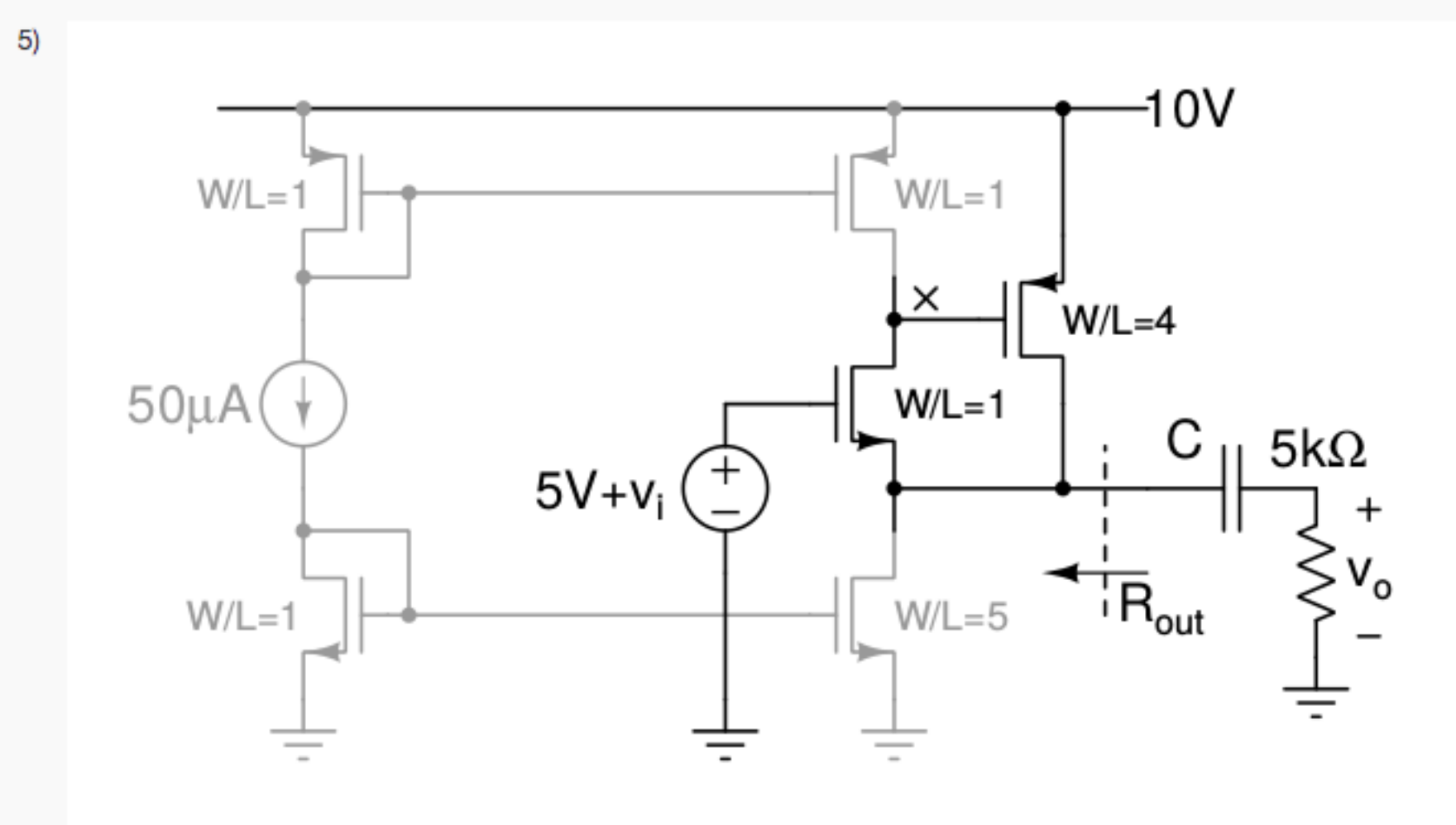
1 point

4) Determine the maximum negative value of v_i for which all transistors remain in the desired region (Same procedure as in the previous question).

(The answer must be in volts (V). Round off fractional answers to one decimal place.)

No, the answer is incorrect.
 Score: 0
 Accepted Answers:
 (Type: Range) -0.34,-0.32

1 point



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 W/L ratios are shown next to respective transistors.
 The capacitor C is very large.

(Same hint as for the first question. If it appears that you have unsolvable conditions in small signal analysis, connect R_x between node x and ground, and take the limit $R_x \rightarrow \infty$.)

Determine the gain v_o/v_i .

(The answer must be the value of the gain. Round off fractional answers to one decimal place.)

No, the answer is incorrect.
 Score: 0
 Accepted Answers:
 (Type: Numeric) 1

1 point

6) Determine the small signal resistance R_{out} .

(The answer must be in kilohms (kΩ). Round off fractional answers to one decimal place.)

No, the answer is incorrect.
 Score: 0
 Accepted Answers:
 (Type: Numeric) 0

1 point

7) Determine the maximum positive value of v_i for which all transistors remain in the desired region, i.e. neither in triode region nor cutoff (For this, you have to calculate the limit on v_i induced by each transistor entering triode region or cutoff and take the worst case).

(The answer must be in volts (V). Round off fractional answers to one decimal place.)

No, the answer is incorrect.
 Score: 0
 Accepted Answers:
 (Type: Numeric) 1.5

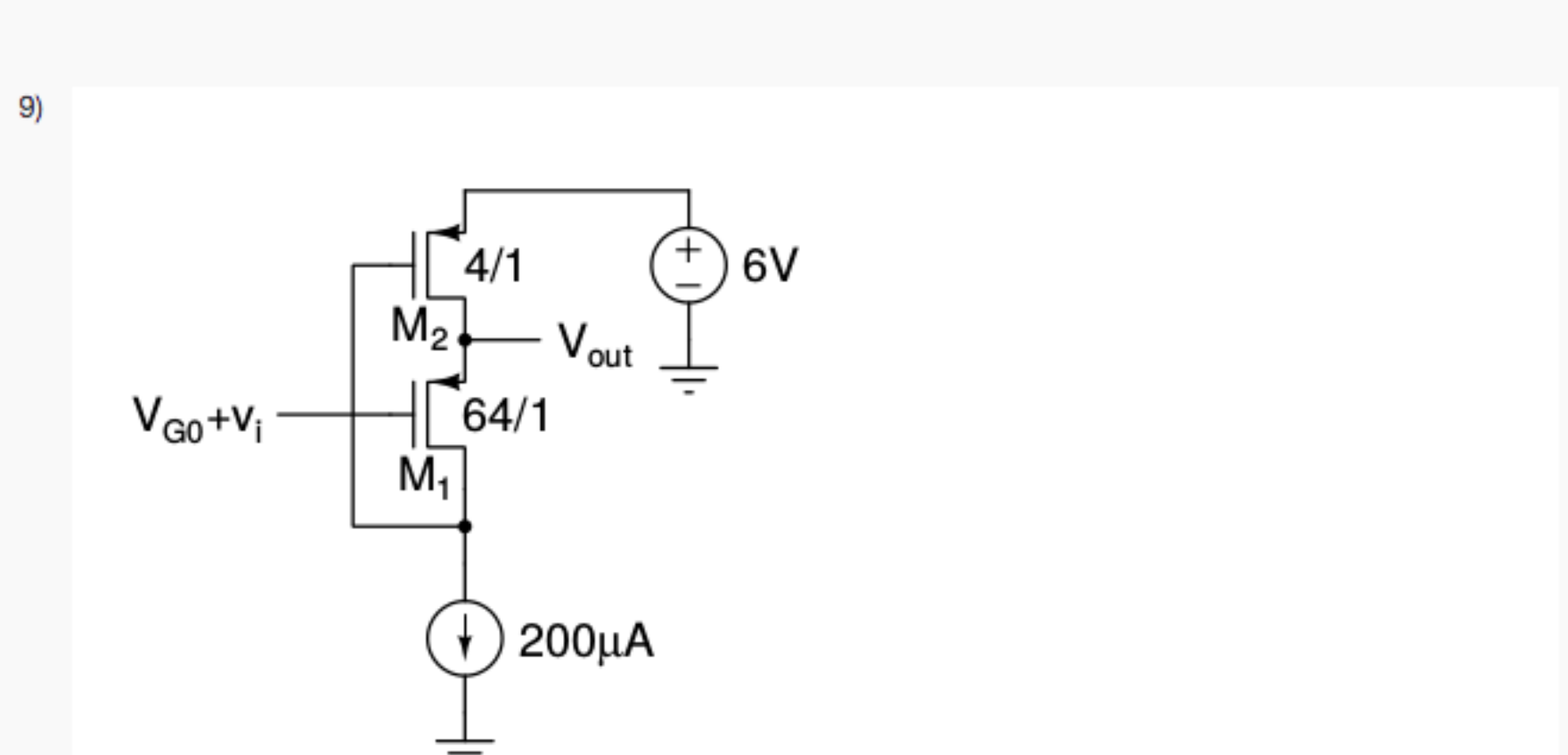
1 point

8) Determine the maximum negative value of v_i for which all transistors remain in the desired region (Same procedure as in the previous question).

(The answer must be in volts (V). Round off fractional answers to one decimal place.)

No, the answer is incorrect.
 Score: 0
 Accepted Answers:
 (Type: Numeric) -1

1 point



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 $\mu_p C_{ox} = 25\mu\text{A}/\text{V}^2$, $V_{Tp} = 1\text{ V}$.
 W/L ratios are shown next to respective transistors.

In the circuit above, the gate of M_1 is driven by a bias voltage V_{G0} plus a sinusoidal input signal $v_i = V_p \cos(\omega t)$. Determine V_{G0} that maximizes V_p that can be applied while keeping all transistors in saturation, and the resulting maximum V_p .

Optimum value of V_{G0} .

(The answer must be in volts (V). Round off fractional answers to two decimal places.)

No, the answer is incorrect.
 Score: 0
 Accepted Answers:
 (Type: Numeric) 2.25

1 point

10) Maximum value of V_p

(The answer must be in volts (V). Round off fractional answers to two decimal places.)

No, the answer is incorrect.
 Score: 0
 Accepted Answers:
 (Type: Numeric) 0.25

1 point