

Unit 8 - Week 6 - Controlled sources continued-VCCS, CCCS, CCVS

Course outline

How does an NPTEL online course work?

Week 0

Week 1 - Obtaining power gain and need for nonlinearity

Week 2 - Nonlinear two ports; MOS transistor; Common source amplifier

Week 3 - Common source amplifier using the MOS transistor

Week 4 - Biasing a MOS transistor at a fixed drain current; CS amplifier using drain feedback bias and current mirror bias

Week 5 - CS amplifier using source feedback bias; Controlled sources using a MOS transistor-VCCS

Week 6 - Controlled sources continued-VCCS, CCCS, CCVS

- VCCS using a MOS transistor
- VCCS using a MOS transistor: Small signal picture
- VCCS using a MOS transistor: Complete circuit
- VCCS using a MOS transistor: AC coupling the output
- Source degenerated CS amplifier
- CCCS using a MOS transistor
- CCCS using a MOS transistor: Small signal picture
- CCCS using a MOS transistor: Complete circuit
- CCVS using a MOS transistor
- CCVS using a MOS transistor: Gain
- CCVS using a MOS transistor: Input and output resistances
- CCVS using a MOS transistor: Complete circuit

Quiz : Assignment 6

- Analog Circuits: Week 6 Feedback form
- Assignment 6 Solutions

Week 7 - Opamp controlled sources; Virtual short; Swing limits; Summary of amplifiers

Week 8 - pMOS transistor; Converting pMOS circuits to nMOS

Week 9 - Common source amplifier with active load; CMOS inverter

Week 10 - Differential pair with current mirror load; Single-stage opamp

Week 11 - Two-stage opamp; Opamp characteristics

Week 12 - Bipolar transistors

Lecture Notes

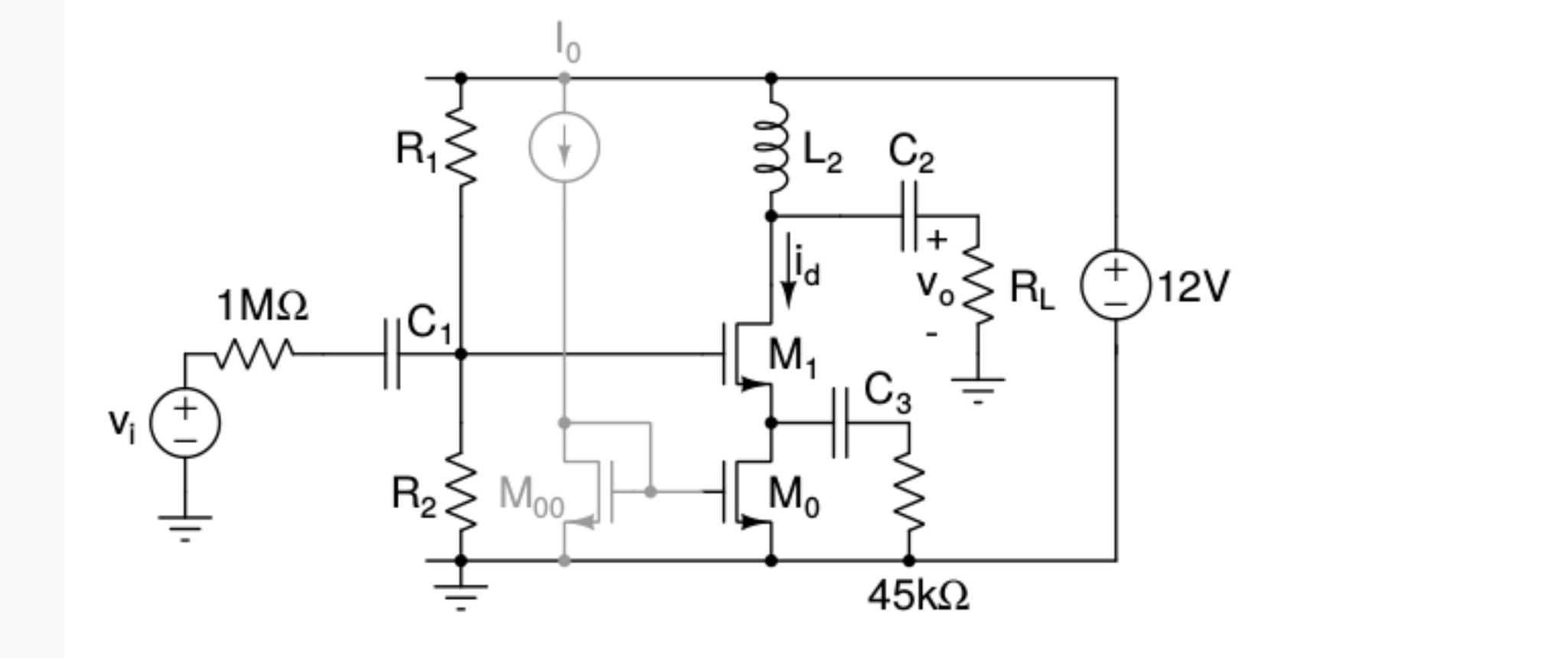
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Assignment 6

The due date for submitting this assignment has passed. **Due on 2020-03-11, 23:59 IST.**
As per our records you have not submitted this assignment.



$\mu_n C_{ox} = 100 \mu A/V^2, W/L = 1, V_T = 1 V.$

The transistor M_1 in the figure above is biased using a current mirror $M_{00} - M_0$. Assuming that C_1, R_1, R_2 are very large, $i_d/v_i = 20 \mu S$. i_d is the small signal drain current. Determine the bias current I_0 . All transistors are in saturation.

(The answer must be in **microamperes (μA)**. Round off fractional answers to one decimal place.)

No, the answer is incorrect.
Score: 0
Accepted Answers: (Type: Numeric) 200

2) In the above circuit, M_0 is on the verge of triode region, i.e. it just meets the condition for saturation. Determine the ratio R_1/R_2 .

(The answer must be the ratio. Round off fractional answers to one decimal place.)

No, the answer is incorrect.
Score: 0
Accepted Answers: (Type: Numeric) 1.4

3) In the above circuit $v_o/v_i = -4$, where v_o is the small signal voltage across R_L . Determine R_L assuming that L_2, C_2 are very large.

(The answer must be in **kilohms (k Ω)**. Round off fractional answers to one decimal place.)

No, the answer is incorrect.
Score: 0
Accepted Answers: (Type: Numeric) 200

4) In the above circuit, with the above value of R_L , determine the condition for L_2 to behave like an open circuit. The signal frequency is 1 MHz.

(The answer must be in **millihenries (mH)**. Round off fractional answers to the nearest integer.)

No, the answer is incorrect.
Score: 0
Accepted Answers: (Type: Numeric) 32

5)

$\mu_n C_{ox} = 100 \mu A/V^2, W/L = 1, V_T = 1 V.$

In the figure above, in the quiescent condition, the drain and gate voltages are equal to each other. The source of the transistor is at 1 V wrt ground. $R_L = R_D$.

Determine the small signal gain v_o/v_i . Assume that all capacitors are very large.

(The answer must be the value of the gain. Round off fractional answers to two decimal places.)

No, the answer is incorrect.
Score: 0
Accepted Answers: (Type: Range) 1.53,1.54

6)

$\mu_n C_{ox} = 100 \mu A/V^2, W/L = 1, V_T = 1 V.$

Determine the small signal gain v_o/v_i in the figure above. Assume that all capacitors are very large.

(The answer must be the value of the gain. Round off fractional answers to one decimal place.)

No, the answer is incorrect.
Score: 0
Accepted Answers: (Type: Range) -7.4,-7.3

7) In the above circuit, $\lambda = 0.05 V^{-1}$. Determine the small signal output resistance R_o (between the drain of M_1 and ground), excluding R_D . Assume that all capacitors are very large.

(The answer must be in **megohms (M Ω)**. Round off fractional answers to one decimal place.)

No, the answer is incorrect.
Score: 0
Accepted Answers: (Type: Numeric) 2.2

8)

$\mu_n C_{ox} = 100 \mu A/V^2, W/L = 1, V_T = 1 V.$

Determine the transimpedance v_o/i_i in the circuit above. Assume that the capacitors are shorts at the signal frequency.

(Think about what the transimpedance would have been if the transistors $g_m \rightarrow \infty$. You should be able to do this just by looking at the circuit. But do cross check by taking the limit of the expression you derived).

(The answer must be in **kilohms (k Ω)**. Round off fractional answers to one decimal place.)

No, the answer is incorrect.
Score: 0
Accepted Answers: (Type: Range) 42.8,42.9

9) Determine the input resistance R_{in} in the circuit above. Assume that the capacitors are shorts at the signal frequency.

(The answer must be in **kilohms (k Ω)**. Round off fractional answers to one decimal place.)

No, the answer is incorrect.
Score: 0
Accepted Answers: (Type: Range) 6.0,6.1

10) Determine the output resistance R_{out} in the circuit above. Assume that the capacitors are shorts at the signal frequency.

(The answer must be in **kilohms (k Ω)**. Round off fractional answers to one decimal place.)

No, the answer is incorrect.
Score: 0
Accepted Answers: (Type: Range) 5.8,5.9