

Unit 7 - Week 5 - CS amplifier using source feedback bias; Controlled sources using a MOS transistor-VCVS

Course outline

How does an NPTEL online course work?

Week 0

Week 1 - Obtaining power gain and need for nonlinearity

Week 2 - Nonlinear two ports; MOS transistor; Common source amplifier

Week 3 - Common source amplifier using the MOS transistor

Week 4 - Biasing a MOS transistor at a fixed drain current; CS amplifier using drain feedback bias and current mirror bias

Week 5 - CS amplifier using source feedback bias; Controlled sources using a MOS transistor-VCVS

- Source feedback biasing
- Common source amplifier with source feedback bias
- Constraints on capacitor values
- Sensing at the drain and feeding back to the source
- Sensing at the source and feeding back to the gate
- Ensuring that transistor is in saturation
- Using a resistor instead of current source for biasing
- Controlled sources using a MOS transistor-Introduction
- Voltage controlled voltage source
- VCVS using a MOS transistor-Complete circuit
- VCVS using a MOS transistor-Small signal picture
- VCVS using a MOS transistor-Complete circuit
- Source follower: Effect of output conductance; Constraints on coupling capacitors

Quiz : Assignment 5

- Analog Circuits: Week 5 Feedback form
- Assignment 5 Solutions

Week 6 - Controlled sources continued-VCVS, CCCS, CCVS

Week 7 - Opamp controlled sources; Virtual short; Swing limits; Summary of amplifiers

Week 8 - pMOS transistor; Converting pMOS circuits to nMOS

Week 9 - Common source amplifier with active load; CMOS inverter

Week 10 - Differential pair with current mirror load; Single-stage opamp

Week 11 - Two-stage opamp; Opamp characteristics

Week 12 - Bipolar transistors

Lecture Notes

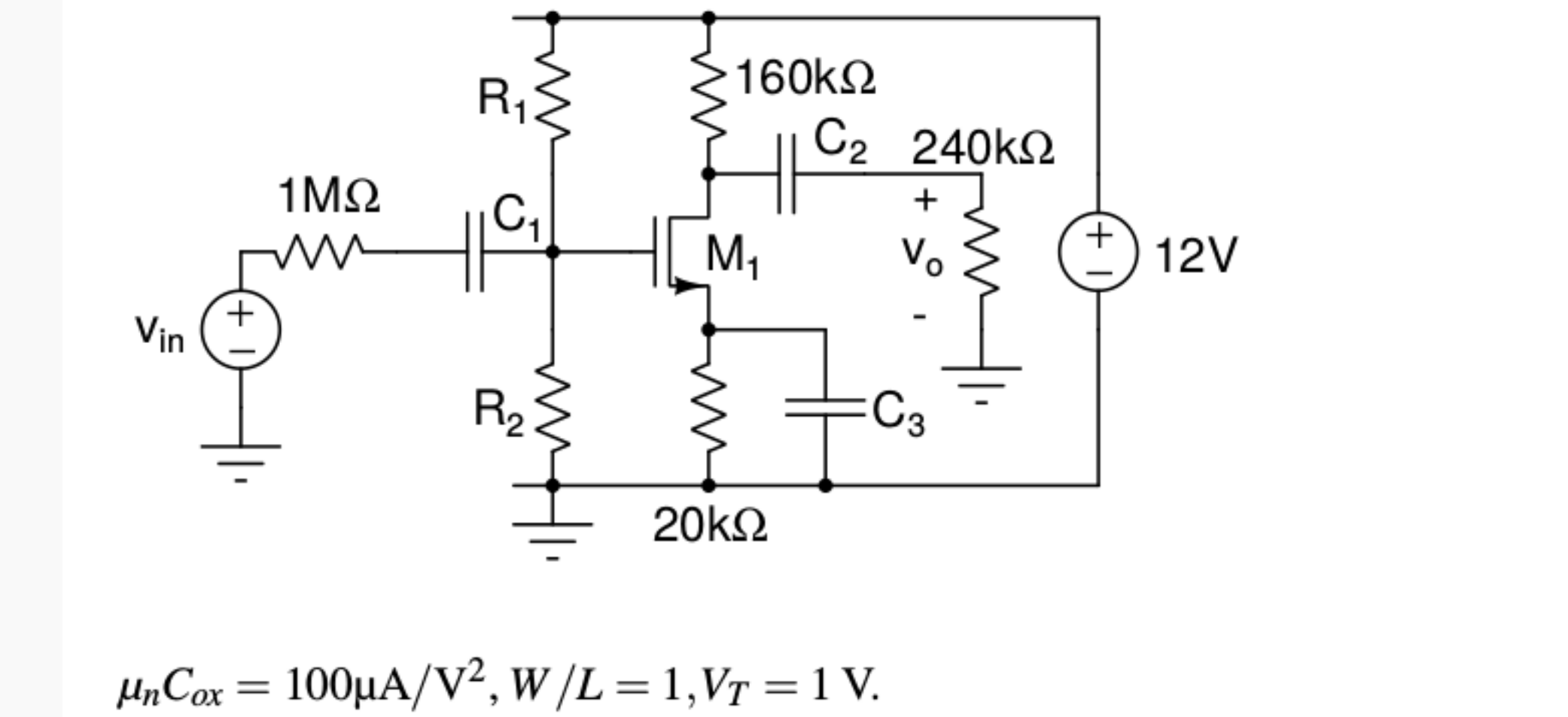
Text Transcripts

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Assignment 5

The due date for submitting this assignment has passed. **Due on 2020-03-04, 23:59 IST.**
As per our records you have not submitted this assignment.



$\mu_n C_{ox} = 100\mu\text{A}/\text{V}^2, W/L = 1, V_T = 1\text{ V}.$

In the above circuit, the operating point current in M_1 is $50\mu\text{A}$, and that in R_1 and R_2 is $1\mu\text{A}$. Determine the following:

Small signal gain v_o/v_{in} assuming that the capacitors are shorts at the signal frequency.

(The answer must be the value of the gain. Round off fractional answers to two decimal places.)

No, the answer is incorrect. Score: 0
Accepted Answers: (Type: Range) -6.65,-6.64

2) Constraint on capacitor C_3 so that it is a short at a signal frequency of 10 kHz . $C_3 \gg C_0$. Determine C_0 . (This constraint is slightly different from that discussed in the lecture because a resistor is used at the source of M_1 for biasing instead of a current source. Re-evaluate the constraint considering the total resistance across the capacitor).

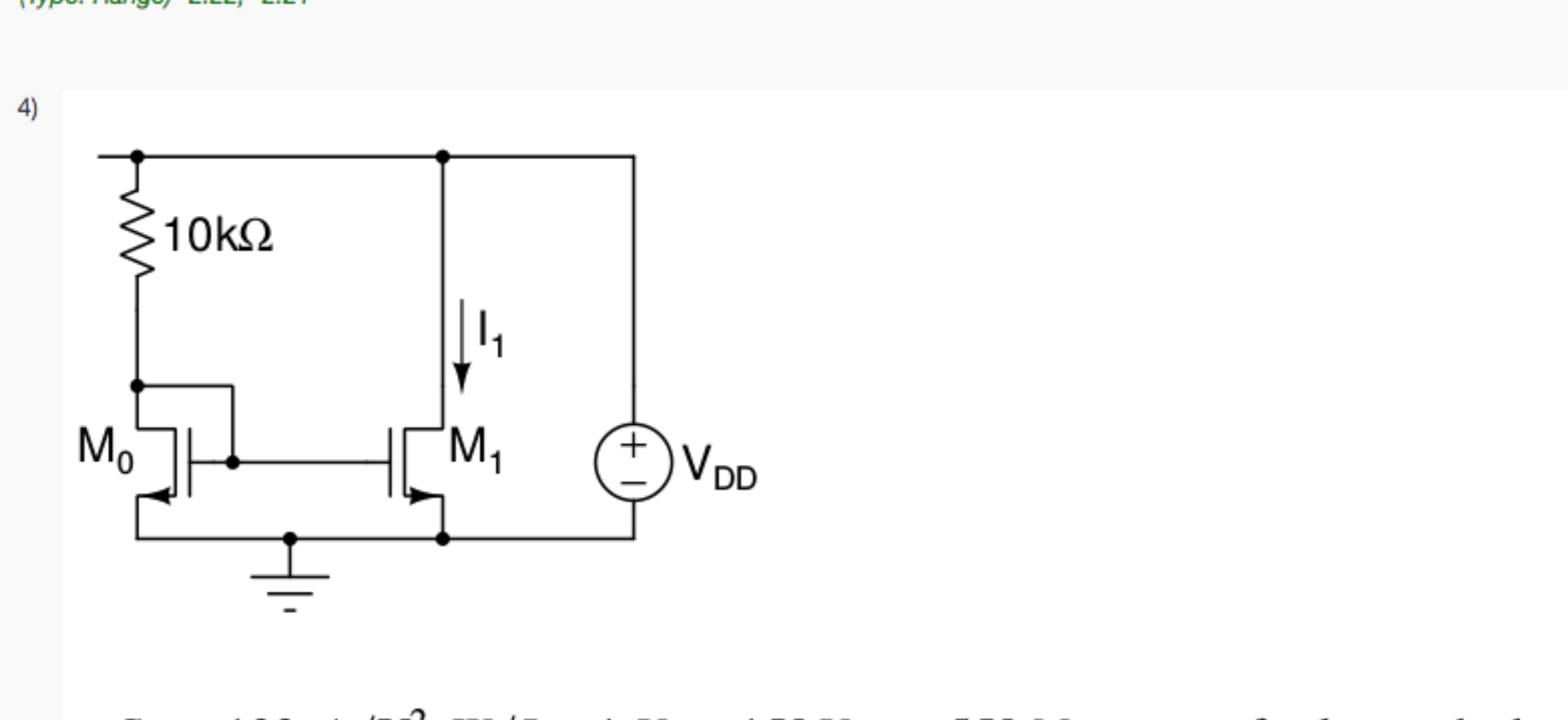
(The answer must be in nanofarads (nF). Round off fractional answers to two decimal places.)

No, the answer is incorrect. Score: 0
Accepted Answers: (Type: Range) 2.38,2.39

3) While constructing the circuit, you forget C_3 altogether. What is the small signal gain v_o/v_{in} assuming that the remaining capacitors are shorts at the signal frequency?

(The answer must be the value of the gain. Round off fractional answers to two decimal places.)

No, the answer is incorrect. Score: 0
Accepted Answers: (Type: Range) -2.22,-2.21



$\mu_n C_{ox} = 100\mu\text{A}/\text{V}^2, W/L = 1, V_T = 1\text{ V}. V_{DD} = 5\text{ V}. M_{0,1}$ are perfectly matched.

Determine the current I_1 .

(The answer must be in microamperes (μA). Round off fractional answers to one decimal place.)

No, the answer is incorrect. Score: 0
Accepted Answers: (Type: Numeric) 200

5) If V_{DD} increases to 5.5 V , determine the increase in I_1 . You can of course re-do the earlier steps. But an easier way is to carry out incremental analysis by representing the change in V_{DD} as a small signal source and using the incremental equivalent circuit of the transistors. (You are encouraged to do both and compare the answers).

Change in I_1 (with appropriate sign; A positive change means a larger I_1 than before).

(The answer must be in microamperes (μA). Round off fractional answers to one decimal place.)

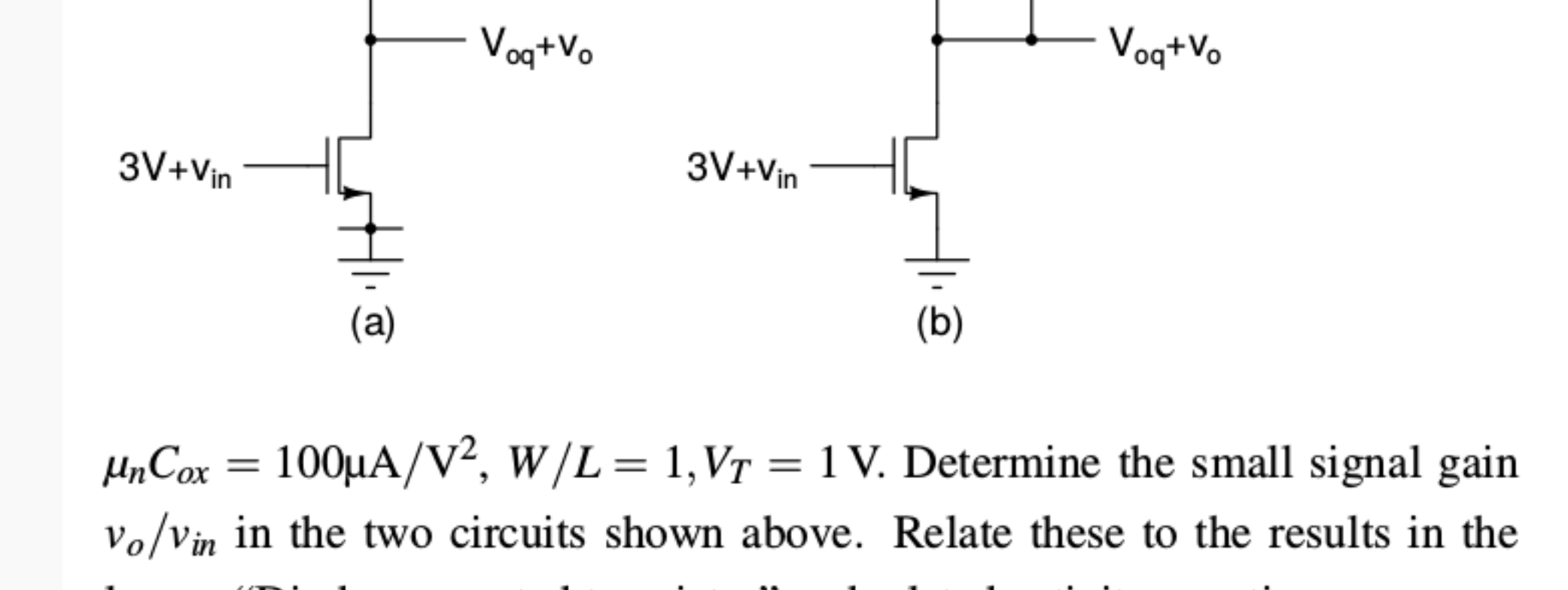
No, the answer is incorrect. Score: 0
Accepted Answers: (Type: Range) 33.3,33.4

6) Assume that $V_{DD} = 10\text{ V}$ and R_D is changed to obtain the same quiescent current as before (with $V_{DD} = 5\text{ V}$ and $R_D = 10\text{ k}\Omega$). Re-evaluate the change in I_1 if V_{DD} increases to 10.5 V . As before, use incremental analysis. Compare the change in this case to that in the earlier case.

Change in I_1 (with appropriate sign; A positive change means a larger I_1 than before).

(The answer must be in microamperes (μA). Round off fractional answers to one decimal place.)

No, the answer is incorrect. Score: 0
Accepted Answers: (Type: Numeric) 12.5



$\mu_n C_{ox} = 100\mu\text{A}/\text{V}^2, W/L = 1, V_T = 1\text{ V}.$ Determine the small signal gain v_o/v_{in} in the two circuits shown above. Relate these to the results in the lesson "Diode connected transistor" and related activity questions.

Small signal gain v_o/v_{in} in (a):

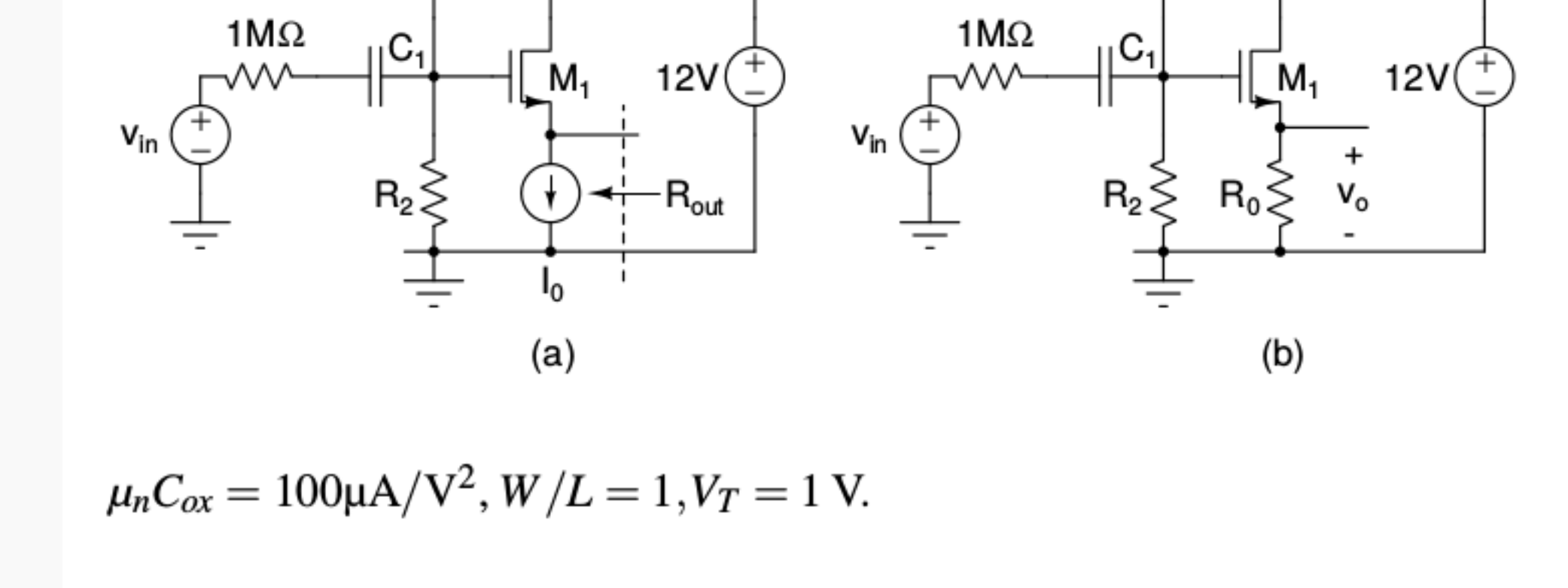
(The answer must be the value of the gain. Round off fractional answers to one decimal place.)

No, the answer is incorrect. Score: 0
Accepted Answers: (Type: Numeric) -1

8) Small signal gain v_o/v_{in} in (b):

(The answer must be the value of the gain. Round off fractional answers to one decimal place.)

No, the answer is incorrect. Score: 0
Accepted Answers: (Type: Numeric) -2



$\mu_n C_{ox} = 100\mu\text{A}/\text{V}^2, W/L = 1, V_T = 1\text{ V}.$

The source follower in (a) is required to have an output resistance of $5\text{ k}\Omega$. Determine the bias current I_0 .

(The answer must be in microamperes (μA). Round off fractional answers to one decimal place.)

No, the answer is incorrect. Score: 0
Accepted Answers: (Type: Numeric) 200

10) The source follower is actually implemented as shown in (b) with a resistor R_0 substituted for the current source. The quiescent voltage across R_0 is specified to be 5 V . Determine the small signal gain v_o/v_i in (b). Assume that C_1, R_1, R_2 are very large.

(The answer must be the value of the gain. Round off fractional answers to two decimal places.)

No, the answer is incorrect. Score: 0
Accepted Answers: (Type: Numeric) 0.83