

# Unit 6 - Week 4 - Biasing a MOS transistor at a fixed drain current; CS amplifier using drain feedback bias and current mirror bias

**Course outline**

How does an NPTEL online course work?

**Week 0**

**Week 1 - Obtaining power gain and need for nonlinearity**

**Week 2 - Nonlinear two ports; MOS transistor; Common source amplifier**

**Week 3 - Common source amplifier using the MOS transistor**

**Week 4 - Biasing a MOS transistor at a fixed drain current; CS amplifier using drain feedback bias and current mirror bias**

- Variation gm with transistor parameters
- Variation of gm with constant VGS and constant drain current bias
- Negative feedback control for constant drain current bias
- Types of feedback for constant drain current bias
- Sense at the drain and feedback to the gate-Drain feedback
- Intuitive explanation of low sensitivity with drain feedback
- Common source amplifier with drain feedback bias
- Constraint on the gate bias resistor
- Constraint on the input coupling capacitor
- Constraint on the output coupling capacitor
- Input and output resistances of the common source amplifier with constant VGS bias
- Current mirror
- Common source amplifier with current mirror bias
- Constraint on coupling capacitors and bias resistance
- Diode connected transistor

**Quiz : Assignment 4**

- Analog Circuits: Week 4 Feedback form
- Assignment 4 Solutions

**Week 5 - CS amplifier using source feedback bias; Controlled sources using a MOS transistor-VCVS**

**Week 6 - Controlled sources continued-VCCS, CCCS, CCVS**

**Week 7 - Opamp controlled sources; Virtual short; Swing limits; Summary of amplifiers**

**Week 8 - pMOS transistor; Converting pMOS circuits to nMOS**

**Week 9 - Common source amplifier with active load; CMOS inverter**

**Week 10 - Differential pair with current mirror load; Single-stage opamp**

**Week 11 - Two-stage opamp; Opamp characteristics**

**Week 12 - Bipolar transistors**

**Lecture Notes**

**Text Transcripts**

**DOWNLOAD VIDEOS**

**Books**

## Assignment 4

The due date for submitting this assignment has passed. **Due on 2020-02-26, 23:59 IST.**  
As per our records you have not submitted this assignment.

1)

$\mu_n C_{ox} = 100\mu\text{A}/\text{V}^2$ ,  $W/L = 1$ ,  $V_T = 1\text{V}$ . The figure above shows a signal source and a load. If a MOS transistor biased in saturation is used between this source and load with no extra components, the gain magnitude must be 24. Determine the bias current which must be flowing through the MOS transistor. (Don't worry about how the operating point is setup. Assume that a MOS transistor at that operating point can be used as a two port amplifier described in this unit.)

(The answer must be in **microamperes ( $\mu\text{A}$ )**. Round off fractional answers to one decimal place.)

No, the answer is incorrect.  
Score: 0  
Accepted Answers: (Type: Numeric) 288

2)

$\mu_n C_{ox} = 100\mu\text{A}/\text{V}^2$ ,  $W/L = 1$ ,  $V_T = 1\text{V}$ . You need to realize the common source amplifier described in the previous problem (with a gain of  $-24$ ) with drain feedback bias arrangement as shown in the above figure (with the value of the bias current determined therein). Determine the constraint on resistor  $R_G$  so that the gain  $v_o/v_s$  is very close to that of just the common source amplifier. (i.e.  $R_G \gg R_0$ , determine  $R_0$ . In this problem, assume that the capacitors are shorts at the signal frequency.)

(The answer must be in **megohms ( $\text{M}\Omega$ )**. Round off fractional answers to two decimal places.)

No, the answer is incorrect.  
Score: 0  
Accepted Answers: (Type: Range) 1.20,1.35

3)

In the above problem, determine the constraint on capacitor  $C_1$ .  $C_1 \gg C_0$ . Determine  $C_0$ . Set the value of  $R_G$  to be 20 times the constraint ( $R_0$ ) evaluated in the previous problem. The signal frequency is at least 1 kHz.

(The answer must be in **picofarads ( $\text{pF}$ )**. Round off fractional answers to the nearest integer.)

No, the answer is incorrect.  
Score: 0  
Accepted Answers: (Type: Range) 140,157

4)

In the above figure, determine the constraint on capacitor  $C_2$ .  $C_2 \gg C_0$ . Determine  $C_0$ . Set the value of  $R_G$  to be 20 times the constraint ( $R_0$ ) evaluated earlier. To evaluate the constraint, use the total resistance that appears across  $C_2$ . The signal frequency is at least 1 kHz.

(The answer must be in **picofarads ( $\text{pF}$ )**. Round off fractional answers to the nearest integer.)

No, the answer is incorrect.  
Score: 0  
Accepted Answers: (Type: Range) 76,86

5)

If  $\lambda$  turns out to be  $0.02\text{V}^{-1}$  in the circuit in the above problem, determine the actual small signal gain of the amplifier you designed above. Assume that  $R_G$ ,  $C_1$ , and  $C_2$  are very large.

(The answer must be the value of the gain. Round off fractional answers to one decimal place.)

No, the answer is incorrect.  
Score: 0  
Accepted Answers: (Type: Range) -15.3,-15.2

6)

$\mu_n C_{ox} = 100\mu\text{A}/\text{V}^2$ ,  $W/L = 1$ ,  $V_T = 1\text{V}$ . Determine the bias current in the transistor in the above figure.

(The answer must be in **microamperes ( $\mu\text{A}$ )**. Round off fractional answers to one decimal place.)

No, the answer is incorrect.  
Score: 0  
Accepted Answers: (Type: Numeric) 50

7)

$\mu_n C_{ox} = 100\mu\text{A}/\text{V}^2$ ,  $W/L = 1$ ,  $V_T = 1\text{V}$ . Determine the small signal resistance  $R_x$  in the above figure.

(The answer must be in **kilohms ( $\text{k}\Omega$ )**. Round off fractional answers to one decimal place.)

No, the answer is incorrect.  
Score: 0  
Accepted Answers: (Type: Numeric) 16

8)

$\mu_n C_{ox} = 100\mu\text{A}/\text{V}^2$ ,  $V_T = 1\text{V}$ .  $M_1$ :  $W/L = 1$ ;  $M_2$ :  $W/L = 4$ . The bias current  $I_0$  is such that the small signal gain  $v_0/v_s = -6$ . Assume that  $C_1$  and  $C_2$  are very large. Determine the power delivered by the 15V voltage source in the quiescent condition.

(The answer must be in **milliwatts ( $\text{mW}$ )**. Round off fractional answers to two decimal places.)

No, the answer is incorrect.  
Score: 0  
Accepted Answers: (Type: Numeric) 3.75

9)

In the above problem, determine the constraint on capacitor  $C_1$ .  $C_1 \gg C_0$ . Determine  $C_0$ . The signal frequency is at least 1 kHz.

(The answer must be in **nanofarads ( $\text{nF}$ )**. Round off fractional answers to two decimal places.)

No, the answer is incorrect.  
Score: 0  
Accepted Answers: (Type: Range) 1.59,1.60

10)

In the above circuit, determine the voltage stored across the capacitor  $C_2$ . (Specifying the magnitude is enough.)

(The answer must be in **volts ( $\text{V}$ )**. Round off fractional answers to one decimal place.)

No, the answer is incorrect.  
Score: 0  
Accepted Answers: (Type: Numeric) 9