

Unit 5 - Week 3 - Common source amplifier using the MOS transistor

Course outline

How does an NPTEL online course work?

Week 0

Week 1 - Obtaining power gain and need for nonlinearity

Week 2 - Nonlinear two ports; MOS transistor; Common source amplifier

Week 3 - Common source amplifier using the MOS transistor

- Basic amplifier structure
- Problems with the basic structure
- Adding bias and signal-ac coupling
- Common source amplifier with biasing
- Common source amplifier: Small signal equivalent circuit
- Common source amplifier analysis: Effect of biasing components
- Constraint on the input coupling capacitor
- Constraint on the output coupling capacitor
- Dependence of ID on VDS
- Small signal output conductance of a MOS transistor
- Effect of gds on a common source amplifier; Inherent gain limit of a transistor

Quiz : Assignment 3

- Analog Circuits: Week 3 Feedback form
- Assignment 3 Solutions

Week 4 - Biasing a MOS transistor at a fixed drain current; CS amplifier using drain feedback bias and current mirror bias

Week 5 - CS amplifier using source feedback bias; Controlled sources using a MOS transistor-VCVS

Week 6 - Controlled sources continued-VCCS, CCCS, CCVS

Week 7 - Opamp controlled sources; Virtual short; Swing limits; Summary of amplifiers

Week 8 - pMOS transistor; Converting pMOS circuits to nMOS

Week 9 - Common source amplifier with active load; CMOS inverter

Week 10 - Differential pair with current mirror load; Single-stage opamp

Week 11 - Two-stage opamp; Opamp characteristics

Week 12 - Bipolar transistors

Lecture Notes

Text Transcripts

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Assignment 3

The due date for submitting this assignment has passed. **Due on 2020-02-19, 23:59 IST.**
As per our records you have not submitted this assignment.

1)

source load

$\mu_n C_{ox} = 100\mu\text{A}/\text{V}^2$, $W/L = 1$, $V_T = 1\text{V}$. The figure above shows a signal source and a load. If a MOS transistor biased in saturation is used between this source and load with no extra components, the gain magnitude must be 8. Determine the bias current which must be flowing through the MOS transistor. (Don't worry about how the operating point is setup. Assume that a MOS transistor at that operating point can be used as a two port amplifier described in this unit.)

(The answer must be in **microamperes (μA)**. Round off fractional answers to one decimal place.)

No, the answer is incorrect.
Score: 0
Accepted Answers: (Type: Numeric) 128

2)

$\mu_n C_{ox} = 100\mu\text{A}/\text{V}^2$, $W/L = 1$, $V_T = 1\text{V}$. The transistor is biased at the current you calculated in the previous problem. The drain bias resistor R_D is chosen to be the same as the load resistance R_L . At the operating point, V_{DS} should be $V_{GS} + 1\text{V}$. The bias current flowing through $R_{1,2}$ must be $10\mu\text{A}$. Determine the following:

Supply voltage V_{DD}

(The answer must be in **volts (V)**. Round off fractional answers to one decimal place.)

No, the answer is incorrect.
Score: 0
Accepted Answers: (Type: Numeric) 10

3)

Small signal gain v_o/v_s in the above figure assuming that the capacitors are very large.

(The answer must be the value of v_o/v_s . Round off fractional answers to two decimal places.)

No, the answer is incorrect.
Score: 0
Accepted Answers: (Type: Range) -2.64,-2.63

4)

Constraint on capacitor C_1 . i.e. $C_1 \gg C_0$. Determine C_0 . (for this constraint, use the total resistance that appears across the capacitor). The signal frequency is 10 kHz.

(The answer must be in **picofarads (pF)**. Round off fractional answers to one decimal place.)

No, the answer is incorrect.
Score: 0
Accepted Answers: (Type: Range) 54.4,54.5

5)

Constraint on capacitor C_2 . i.e. $C_2 \gg C_0$. Determine C_0 . (for this constraint, use the total resistance that appears across the capacitor). The signal frequency is 10 kHz.

(The answer must be in **picofarads (pF)**. Round off fractional answers to the nearest integer.)

No, the answer is incorrect.
Score: 0
Accepted Answers: (Type: Range) 159,160

6)

$\mu_n C_{ox} = 100\mu\text{A}/\text{V}^2$, $W/L = 1$, $V_T = 1\text{V}$. The figure above shows a possible arrangement where the ac coupling capacitors can be eliminated. Determine R_D such that the quiescent drain voltage is zero (i.e. the voltage between drain and ground consists of only the component due to the signal). v_s is a (small) signal source.

(The answer must be in **kilohms (kΩ)**. Round off fractional answers to one decimal place.)

No, the answer is incorrect.
Score: 0
Accepted Answers: (Type: Numeric) 15

7)

Small signal gain v_o/v_s obtained in the above case.

(The answer must be the value of v_o/v_s . Round off fractional answers to one decimal place.)

No, the answer is incorrect.
Score: 0
Accepted Answers: (Type: Numeric) -3

8)

$\mu_n C_{ox} = 100\mu\text{A}/\text{V}^2$, $W/L = 1$, $V_T = 1\text{V}$.

The above circuit must be designed to have a small signal gain of -4 . $R_1, R_2 \gg 100\text{k}\Omega$. The drain bias resistor R_D is chosen to be the same as the load resistance R_L . At the operating point, V_{DS} should be $V_{GS} + 1\text{V}$. The supply voltage V_{DD} must be found such that the above conditions are satisfied.

You have carried out the design assuming that $\lambda = 0$. Now you realize that $\lambda = 0.0625\text{V}^{-1}$. What is the actual small signal gain v_o/v_s ?

(The answer must be the value of the gain. Round off fractional answers to two decimal places.)

No, the answer is incorrect.
Score: 0
Accepted Answers: (Type: Numeric) -3.33

9)

In the above circuit, you have to modify R_D and the supply voltage so that the small signal gain is restored to the original value of -4 .

Value of drain bias resistor R_D :

(The answer must be in **kilohms (kΩ)**. Round off fractional answers to two decimal places.)

No, the answer is incorrect.
Score: 0
Accepted Answers: (Type: Range) 83.32,83.36

10)

Supply voltage V_{DD} :

(The answer must be in **volts (V)**. Round off fractional answers to two decimal places.)

No, the answer is incorrect.
Score: 0
Accepted Answers: (Type: Range) 14.26,14.27