Unit 13 - Week 11 - Two-stage opamp; Opamp characteristics

Course outline

- How does an NPTEL online course work?
- Week 0
- Week 1 - Obtaining power gain and need for nonlinearity
- Week 2 - Nonlinear two ports; MOS transistor; Common source amplifier
- Week 3 - Common source amplifier using the MOS transistor
- Week 4 - Biasing a MOS transistor at a fixed drain current; CS amplifier using drain feedback bias and current mirror bias
- Week 5 - CS amplifier using source feedback bias; Controlled sources using a MOS transistor-VCVS
- Week 6 - Controlled sources continued-VCCS, CCCS, CCVS
- Week 7 - Opamp controlled sources; Virtual short; Swing limits; Summary of amplifiers
- Week 8 - pMOS transistor; Converting pMOS circuits to nMOS
- Week 9 - Common source amplifier with active load; CMOS inverter
- Week 10 - Differential pair with current mirror load; Single-stage opamp
- Week 11 - Two-stage opamp; Opamp characteristics
  - Which transistor type to use for the second stage?
  - Small signal gain
  - DC negative feedback biasing of all stages
  - DC negative feedback biasing of all stages, cont'd
  - Small signal model
  - Swing limits
  - Systematic offset; How to eliminate it
  - Quiz : Assignment 11
  - Analog Circuits: Week 11 Feedback form
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- Week 12 - Bipolar transistors
- Lecture Notes
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- Books

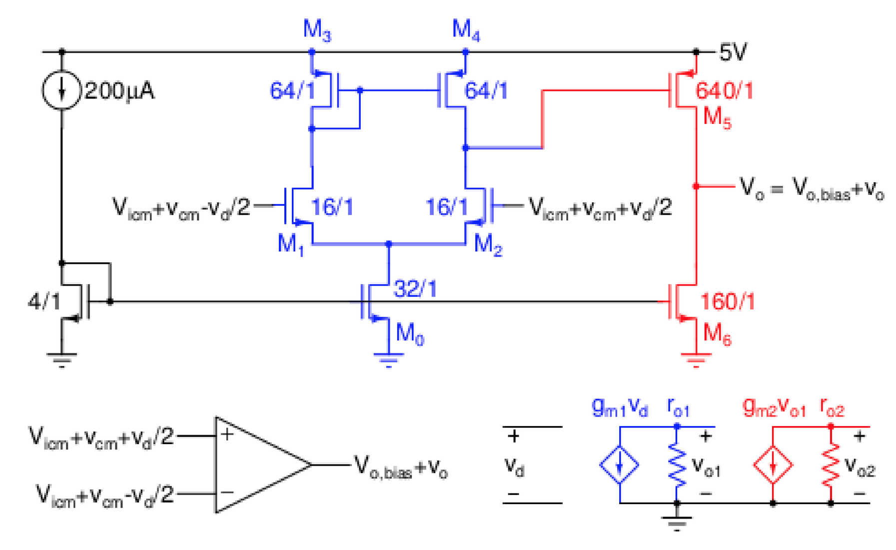
Assignment 11

The due date for submitting this assignment has passed.
As per our records you have not submitted this assignment.

Due on 2020-04-15, 23:59 IST.

1)

$\mu_p C_{ox} = 100\mu A/V^2$, $V_{Tp} = 0.5\,V$, $\lambda_p = 0.05\,V^{-1}$.
$\mu_n C_{ox} = 400\mu A/V^2$, $V_{Tn} = 0.5\,V$, $\lambda_n = 0.05V^{-1}$.



The circuit above is a two-stage opamp. V_{icm}, v_d and v_{cm} are the input common-mode bias voltage, small signal incremental differential input, and small-signal incremental common-mode input respectively. V_o, $V_{o,bias}$, and v_o are the total output voltage, output bias voltage, and the small signal incremental output voltage respectively. The questions below relate to this opamp.

Proceed systematically by first determining the operating point (I_D, V_{GS}, and V_{DS}) and small signal parameters (g_m and g_{ds}) of all transistors. For this, assume that all transistors are operating in saturation region. Use the small signal parameters in the model above. You will need these to answer the questions below.

Determine the upper limit on V_{icm} for all transistors to be in saturation. Small signal inputs are zero.

(The answer must be **in volts (V)**. Round off fractional answers to two decimal places.)

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 4.5

1 point

2)

Determine the lower limit on V_{icm} for all transistors to be in saturation. Small signal inputs are zero.

(The answer must be **in volts (V)**. Round off fractional answers to two decimal places.)

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 1.5

1 point

3)

Determine the upper limit on V_o for all transistors to be in saturation. Neglect small signal input v_d in these calculations.

(The answer must be **in volts (V)**. Round off fractional answers to two decimal places.)

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 4.5

1 point

4)

Determine the lower limit on V_o for all transistors to be in saturation. Neglect small signal input v_d in these calculations.

(The answer must be **in volts (V)**. Round off fractional answers to two decimal places.)

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 0.5

1 point

5)

Determine the differential gain v_o/v_d. $v_{cm} = 0$. Assume that all transistors are in saturation region. For simplicity, set $\lambda_n = 0$ for M_0.

(The answer must be **value of the gain**. Round off fractional answers to one decimal place.)

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 1600

1 point

6)

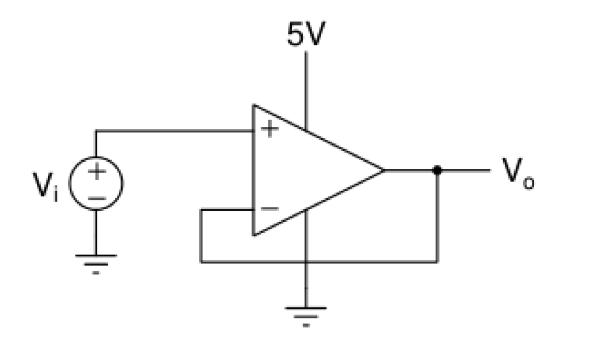
Determine the common mode gain v_o/v_{cm}. $v_d = 0$. Assume that all transistors are in saturation region. For simplicity, set $\lambda = 0$ for M_{1-4}.

(The answer must be **value of the gain**. Round off fractional answers to two decimal places.)

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Range) 0.45,0.55

1 point

7)



The two-stage opamp shown earlier is used to realize a unity gain voltage follower. The input $V_i = V_{i,bias} + V_p\cos(\omega t)$. $V_{i,bias}$ is adjusted so that the amplitude V_p which can be applied is maximized.

Determine the optimum bias $V_{i,cm}$.

(The answer must be **in volts (V)**. Round off fractional answers to three decimal places.)

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 3

1 point

8)

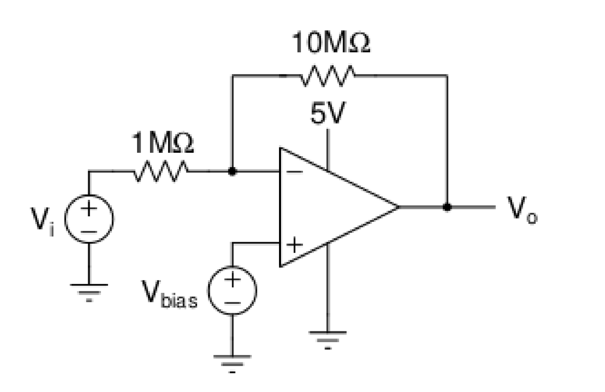
Determine the maximum V_p that can be applied.

(The answer must be **in volts (V)**. Round off fractional answers to three decimal places.)

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 1.5

1 point

9)



The two-stage opamp shown earlier is used to realize an inverting amplifier shown above. The input $V_i = V_{bias} + V_p\cos(\omega t)$. V_{bias} is adjusted so that the amplitude V_p which can be applied is maximized.

Determine the optimum bias V_{bias}. (First analyze the circuit assuming an ideal opamp. You can then apply the swing limit constraints on the input common mode and the output voltages).

(The answer must be **in volts (V)**. Round off fractional answers to two decimal places.)

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 2.5

1 point

10)

Determine the maximum V_p that can be applied.

(The answer must be **in millivolts (mV)**. Round off fractional answers to one decimal place.)

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 200

1 point