Unit 12 - Week 10 - Differential pair with current mirror load; Single-stage opamp

Course outline

How does an NPTEL online course work?

Week 0

Week 1 - Obtaining power gain and need for nonlinearity

Week 2 - Nonlinear two ports; MOS transistor; Common source amplifier

Week 3 - Common source amplifier using the MOS transistor

Week 4 - Biasing a MOS transistor at a fixed drain current; CS amplifier using drain feedback bias and current mirror bias

Week 5 - CS amplifier using source feedback bias; Controlled sources using a MOS transistor-VCVS

Week 6 - Controlled sources continued-VCCS, CCCS, CCVS

Week 7 - Opamp controlled sources; Virtual short; Swing limits; Summary of amplifiers

Week 8 - pMOS transistor; Converting pMOS circuits to nMOS

Week 9 - Common source amplifier with active load; CMOS inverter

Week 10 - Differential pair with current mirror load; Single-stage opamp

- Amplifying a difference signal; Differential pair
- Differential pair-small signal basics
- Biasing a differential pair
- Differential pair with differential excitation
- Differential pair with a current mirror load
- Differential pair with a current mirror load-operating point
- Differential pair with a current mirror load-Norton equivalent current
- Differential pair with a current mirror load-Norton equivalent resistance
- Common mode gain
- Single stage opamp
- Single stage opamp: Input common mode swing limits
- Single stage opamp: Output swing limits
- Quiz : Assignment 10
- Analog Circuits: Week 10 Feedback form
- Assignment 10 Solutions

Week 11 - Two-stage opamp; Opamp characteristics

Week 12 - Bipolar transistors

Lecture Notes

Text Transcripts

DOWNLOAD VIDEOS

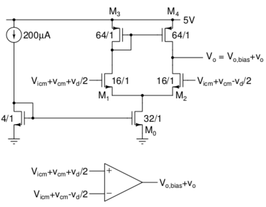
Books

Assignment 10

The due date for submitting this assignment has passed.
As per our records you have not submitted this assignment.

Due on 2020-04-08, 23:59 IST.

1) M_p: $\mu_p C_{ox} = 100\mu A/V^2$, $V_{Tp} = 0.5\,V, \lambda_p = 0.05\,V^{-1}$.
M_n: $\mu_n C_{ox} = 400\mu A/V^2$, $V_{Tn} = 0.5\,V, \lambda_n = 0.05\,V^{-1}$



The circuit above is a single stage opamp. V_{icm}, v_d and v_{cm} are the input common-mode bias voltage, small signal incremental differential input, and small-signal incremental common-mode input respectively. V_o, $V_{o,bias}$, and v_o are the total output voltage, output bias voltage, and the small signal incremental output voltage respectively.

Determine the upper limit on V_{icm} for all transistors to be in saturation. Small signal inputs are zero.

(The answer must be **in volts (V)**. Round off fractional answers to two decimal places.)

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 4.5

1 point

2) Determine the lower limit on V_{icm} for all transistors to be in saturation. Small signal inputs are zero.

(The answer must be **in volts (V)**. Round off fractional answers to two decimal places.)

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 1.5

1 point

3) Determine the upper limit on V_o for all transistors to be in saturation. Small signal inputs are zero.

(The answer must be **in volts (V)**. Round off fractional answers to two decimal places.)

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 4.5

1 point

4) Determine the lower limit on V_o for all transistors to be in saturation. Small signal inputs are zero. Assume that $V_{i,cm}$ is in the middle of the range determined above.

(The answer must be **in volts (V)**. Round off fractional answers to two decimal places.)

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 2.5

1 point

5) Determine the differential gain v_o/v_d. $v_{cm} = 0$. Assume that all transistors are in saturation region. For simplicity, you can set $\lambda_n = 0$ for M_0.

(The answer must be **value of the gain**. Round off fractional answers to one decimal place.)

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Range) 39,41

1 point

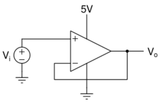
6) Determine the common mode gain v_o/v_{cm}. $v_d = 0$. Assume that all transistors are in saturation region. For simplicity, you can set $\lambda_n = 0$ for all transistors other than M_0.

(The answer must be **value of the gain**. Round off fractional answers to three decimal places.)

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) -0.012

1 point

7)



The single-stage opamp shown earlier is used to realize a unity gain voltage follower. The input $V_i = V_{i,bias} + V_p \cos(\omega t)$. $V_{i,bias}$ is adjusted so that the amplitude V_p which can be applied is maximized.

Determine the optimum bias $V_{i,cm}$.

(The answer must be **in volts (V)**. Round off fractional answers to two decimal places.)

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 3

1 point

8) Determine the maximum V_p that can be applied.

(The answer must be **in volts (V)**. Round off fractional answers to two decimal places.)

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Numeric) 1.5

1 point

9) Determine the small signal gain when the input is set to the optimum bias. Don't approximate this to unity. Use the actual gain of the opamp.

(The answer must be **value of the gain**. Round off fractional answers to three decimal places.)

No, the answer is incorrect.
Score: 0
Accepted Answers:
(Type: Range) 0.97,0.98

1 point

10) If the supply voltage of the unity gain voltage follower is increased,

1 point

- Both the upper and lower swing limits on V_i change
- Neither the upper nor the lower swing limit on V_i changes.
- The upper swing limit changes, but the lower swing limit does not change
- The upper swing limit does not change, but the lower swing limit changes

No, the answer is incorrect.
Score: 0
Accepted Answers:
The upper swing limit changes, but the lower swing limit does not change