Unit 11 - WEEK 9

Week 9 Assignment 9

The due date for submitting this assignment has passed.
As per our records you have not submitted this assignment.

Due on 2020-04-01, 23:59 IST.

Common data for Q 9.1 to Q 9.6:

The circuit shown in Fig 9.1 is a single stage fully differential amplifier.

The values of device parameters for both transistors are given as:
$\beta_1 = \beta_2 = 200$, $V_{BE(on)1} = V_{BE(on)2} \approx 0.6$ V, $V_{CE(sat)1} = V_{CE(sat)2} \approx 0.3$ V. Assume, early voltages of both transistors are $V_{A1} = V_{A2} = 100$ V.

The values of the components in the differential amplifier circuit are given as:
$R_{C1} = R_{C2} = 4.7$ kΩ, $R_T = 1$ kΩ.

The power supply, $V_{CC} = 12$V and the input common mode bias voltage, $V_{INC} = 3$ V.
Consider thermal equivalent voltage, $V_T = 26$ mV.

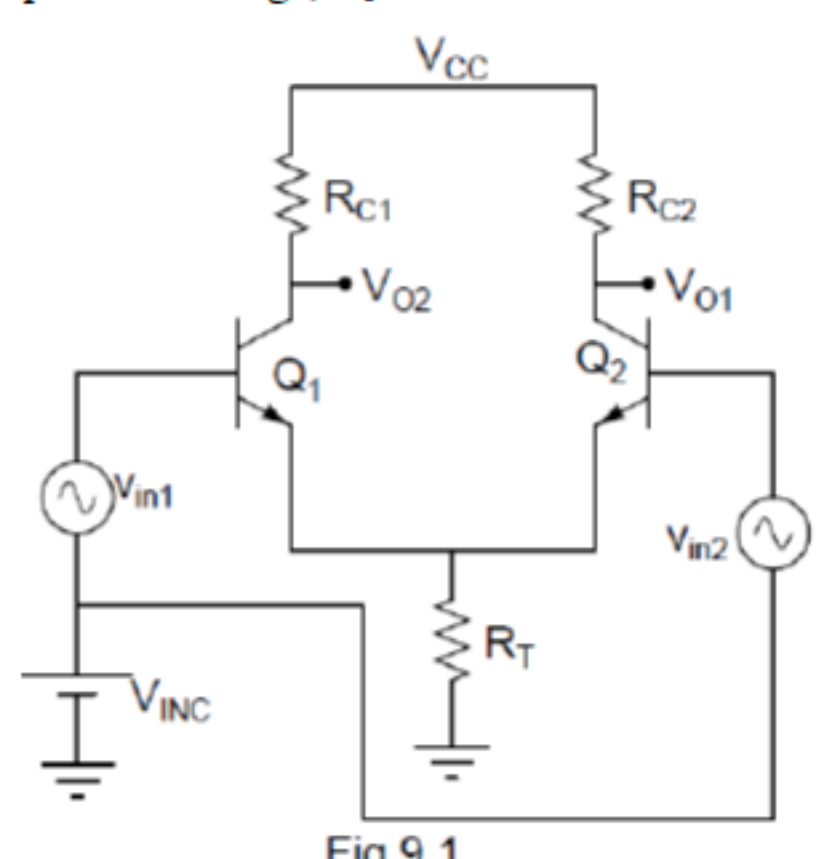

Fig 9.1

1) Refer to the circuit shown in Fig 9.1, find the DC voltage ($V_{O1} = V_{O2} = V_{O\_DC}$) between collector of Q_1 (or Q_2) and ground. Select the closest option from the following: *2 points*

a) 4.95 V b) 6.36 V c) 3.54 V d) 2.7 V e) 5.64 V

- a)
- b)
- c)
- d)
- e)

No, the answer is incorrect.
Score: 0
Accepted Answers:
b)

2) Refer to the circuit shown in Fig 9.1, find the maximum output voltage swing (without having significant distortion) in positive direction (w.r.t DC level) for a sinusoidal input signal. Select the closest option from the following: *1 point*

a) 4.95 V b) 6.36 V c) 3.54 V d) 2.7 V e) 5.64 V

- a)
- b)
- c)
- d)
- e)

No, the answer is incorrect.
Score: 0
Accepted Answers:
e)

3) Find the differential mode gain of the differential amplifier circuit as shown in Fig 9.1. Select the closest option from the following: *1 point*

a) 217 b) 108 c) 434 d) 2.3 e) 93.5

- a)
- b)
- c)
- d)
- e)

No, the answer is incorrect.
Score: 0
Accepted Answers:
a)

4) Find the common mode gain of the differential amplifier circuit as shown in Fig 9.1. Select the closest option from the following: *1 point*

a) – 217 b) – 108 c) – 4.6 d) – 2.3 e) – 93.5

- a)
- b)
- c)
- d)
- e)

No, the answer is incorrect.
Score: 0
Accepted Answers:
d)

5) Find the differential output signal ($v_{o\_d} = v_{o1} - v_{o2}$) for the differential amplifier circuit as shown in Fig 9.1. The input signals for the differential amplifier circuit are given as: *2 points*

$v_{in1} = 0.005 \sin\left(\frac{2\pi}{T}t\right) + 0.3 \sin\left(\frac{2\pi}{8T}t\right)$ V, $v_{in2} = -0.005 \sin\left(\frac{2\pi}{T}t\right) + 0.3 \sin\left(\frac{2\pi}{8T}t\right)$ V.

Select the closest option from the following:

a) $4.34 \sin\left(\frac{2\pi}{8T}t\right)$ V b) $2.17 \sin\left(\frac{2\pi}{8T}t\right)$ V c) $2.17 \sin\left(\frac{2\pi}{T}t\right)$ V
d) $1.08 \sin\left(\frac{2\pi}{8T}t\right)$ V e) $1.08 \sin\left(\frac{2\pi}{T}t\right)$ V f) $4.34 \sin\left(\frac{2\pi}{T}t\right)$ V

- a)
- b)
- c)
- d)
- e)
- f)

No, the answer is incorrect.
Score: 0
Accepted Answers:
c)

6) Find the output voltage signal (v_{o1}) for the differential amplifier circuit as shown in Fig 9.1. The input signals for the differential amplifier circuit are given as: *2 points*

$v_{in1} = 0.005 \sin\left(\frac{2\pi}{T}t\right) + 0.3 \sin\left(\frac{2\pi}{8T}t\right)$ V, $v_{in2} = -0.005 \sin\left(\frac{2\pi}{T}t\right) + 0.3 \sin\left(\frac{2\pi}{8T}t\right)$ V.

Select the closest option from the following:

a) $2.17 \sin\left(\frac{2\pi}{T}t\right) - 0.69 \sin\left(\frac{2\pi}{8T}t\right)$ V b) $2.17 \sin\left(\frac{2\pi}{T}t\right) + 0.69 \sin\left(\frac{2\pi}{T}t\right)$ V
c) $1.08 \sin\left(\frac{2\pi}{T}t\right) + 0.69 \sin\left(\frac{2\pi}{8T}t\right)$ V d) $1.08 \sin\left(\frac{2\pi}{T}t\right) - 0.69 \sin\left(\frac{2\pi}{8T}t\right)$ V
e) $-1.08 \sin\left(\frac{2\pi}{T}t\right) - 0.69 \sin\left(\frac{2\pi}{8T}t\right)$ V f) $-1.08 \sin\left(\frac{2\pi}{T}t\right) + 0.69 \sin\left(\frac{2\pi}{8T}t\right)$ V

- a)
- b)
- c)
- d)
- e)
- f)

No, the answer is incorrect.
Score: 0
Accepted Answers:
d)

Common data for Q 9.7 to Q 9.8

The circuit shown in Fig 9.2 is a single stage fully differential amplifier.

The values of device parameters for both transistors are given as:
$K\frac{W}{L} = 1$ mA/V^2, $V_{th} = 1$ V, $\lambda = 0.01$ V^{-1}.

The values of the components in the amplifier are given as:
$R_{D1} = R_{D2} = 2$ kΩ, $R_T = 1$ kΩ.

The supply voltage $V_{DD} = 12$ V and the input common mode bias voltage $V_{INC} = 7$ V.

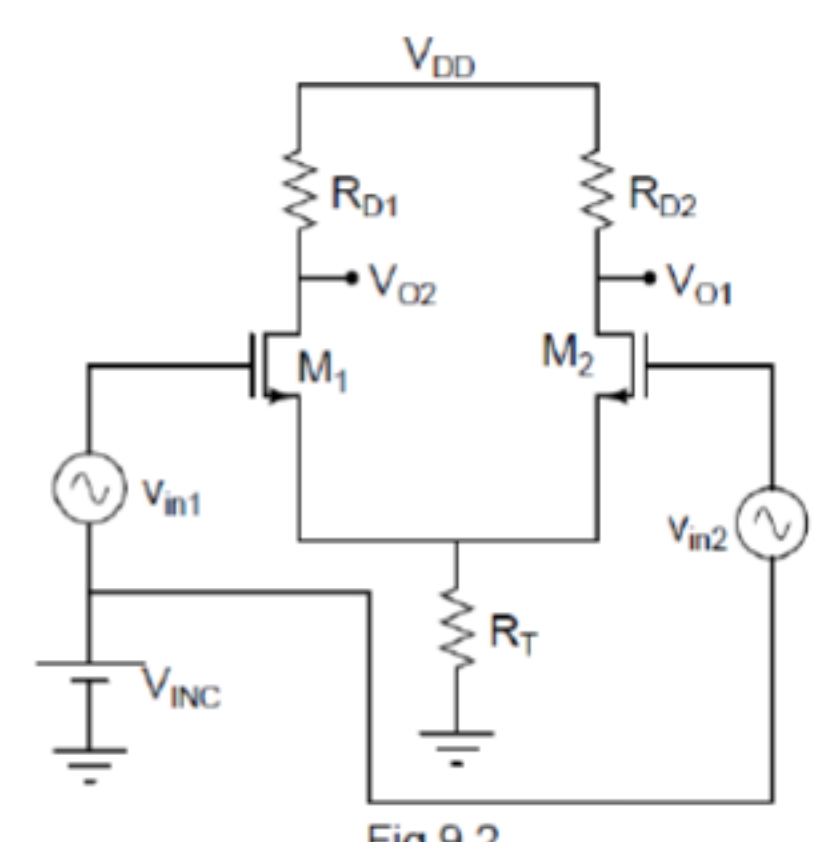

Fig 9.2

7) Refer to the circuit in Fig 9.2, find the DC voltage ($V_{O1} = V_{O2} = V_{O\_DC}$) between drain of M_1 (or M_2) and ground. Select the closest option from the following: *2 points*

a) 8 V b) 6 V c) 4 V d) 10 V e) 5 V

- a)
- b)
- c)
- d)
- e)

No, the answer is incorrect.
Score: 0
Accepted Answers:
a)

8) Find the Common Mode Rejection Ratio (CMRR) of the differential amplifier circuit as shown in Fig 9.2. Select the closest option from the following: *2 points*

[*Hint:* CMRR = $\frac{|A_d|}{|A_C|}$
A_d: Differential mode gain of the differential amplifier
A_C: Common mode gain of the differential amplifier]

a) 2 b) 4 c) 5 d) 0.8 e) 0.4

- a)
- b)
- c)
- d)
- e)

No, the answer is incorrect.
Score: 0
Accepted Answers:
c)

Common data for Q 9.9 to Q 9.11

The circuit shown in Fig 9.3 is a single stage fully differential amplifier.

The values of device parameters for transistors are given as:
$K\left(\frac{W}{L}\right)_2 = K\left(\frac{W}{L}\right)_3 = 0.75$ mA/V^2, $V_{th2} = V_{th3} = 1$ V, $\lambda_2 = \lambda_3 = 0.01$ V^{-1}, $V_{BE(on)1} \approx 0.6$ V, $V_{CE(Sat)1} \approx 0.3$ V, $\beta_1 = 150$, $V_{A1} = 120$ V.
The values of the components in the amplifier are given as:
$R_{D1} = R_{D2} = 3$kΩ, $R_{B1} = 570$ kΩ.

The supply voltage $V_{DD} = 12$ V. The value of V_{INC} is such that both M_2 and M_3 transistors are operating in saturation region and Q_1 is in active region.

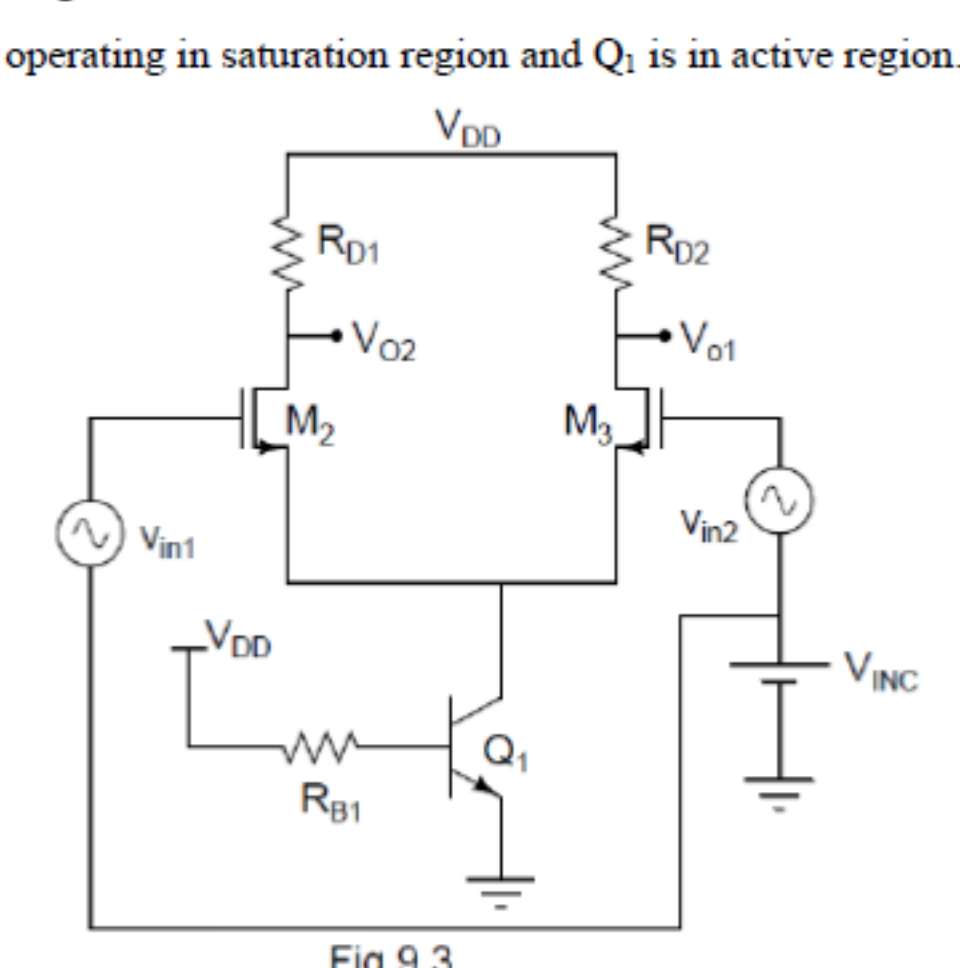

Fig 9.3

9) Refer to the circuit shown in Fig 9.3, find the DC voltage ($V_{O1} = V_{O2} = V_{O\_DC}$) between drain of M_2 (or M_3) and ground. Select the closest option from the following: *2 points*

a) 4.5 V b) 3 V c) 9 V d) 6 V e) 7.5 V

- a)
- b)
- c)
- d)
- e)

No, the answer is incorrect.
Score: 0
Accepted Answers:
e)

10) Find the range of input common mode DC voltage (V_{INC}) such that both M_2 and M_3 transistors are operating in saturation region and Q_1 is in active region for the differential amplifier circuit as shown in Fig 9.3. Select the closest option from the following: *2 points*

a) 3.3 V ≤ V_{INC} ≤ 7.5 V b) 2.7 V ≤ V_{INC} ≤ 8.5 V
c) 2.7 V ≤ V_{INC} ≤ 7.5 V d) 3.3 V ≤ V_{INC} ≤ 6.5 V
e) 2.7 V ≤ V_{INC} ≤ 6.5 V f) 3.3 V ≤ V_{INC} ≤ 8.5 V

- a)
- b)
- c)
- d)
- e)
- f)

No, the answer is incorrect.
Score: 0
Accepted Answers:
f)

11) Find the Common Mode Rejection Ratio (CMRR) of the differential amplifier circuit as shown in Fig 9.3. Select the closest option from the following: *2 points*

a) 4.5 b) 121 c) 0.04 d) 61 e) 241

- a)
- b)
- c)
- d)
- e)

No, the answer is incorrect.
Score: 0
Accepted Answers:
b)

12) The advantage of using active device over passive element (say, resistor) to generate the tail current in a differential amplifier is / are the following: *1 point*

(a) Input common mode voltage range is increased
(b) Common mode gain is increased
(c) Common mode gain is decreased
(d) Differential mode gain is increased
(e) Differential mode gain is decreased

- a)
- b)
- c)
- d)
- e)

No, the answer is incorrect.
Score: 0
Accepted Answers:
a)
c)