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NPTEL (https://swayam.gov.in/explorer?ncCode=NPTEL) » Architectural Design of Digital Integrated Circuits (course)

Announcements (announcements)

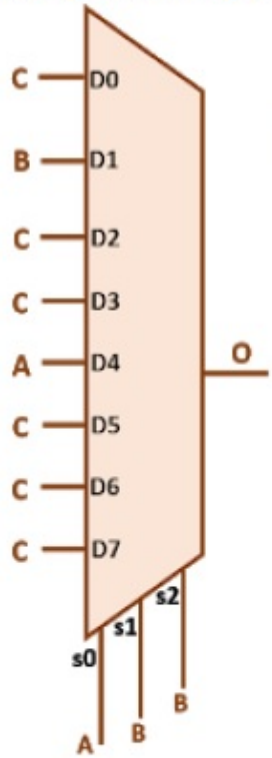
About the Course (https://swayam.gov.in/nd1_noc20_ee37/preview) Ask a Question (forum)

Progress (student/home) Mentor (student/mentor)

Due on 2020-04-24, 23:59 IST

1. A) Negative gate delay - is it possible in the digital circuits or not.
   B) Explain Latency and throughput – the two measures of system performance.

2. Explain need along with the working principle of Reset Synchronizer?
3. A) What is clock multiplexer? Design a circuit for glitch free clock switching between two synchronous clocks.
   B) Given an 8:1 multiplexer such that the input connected to 5th input is the most setup timing critical and other inputs are timing critical in the order D0 > D1 > D2 > D3 > D4 > D6 > D7. Restructure the logic accordingly.
4. An 8:1 multiplexer selects one out of three inputs based upon different combinations of S2, S1 and S0 as shown in figure below. Minimize the logic with a view that B is the most timing critical input



S2	S1	S0	O
0	0	0	C
0	0	1	B
0	1	0	C
0	1	1	C
1	0	0	A
1	0	1	C
1	1	0	C
1	1	1	C

5. A) How do you detect if two 8-bit numbers/signals are equal.

   B) Design a circuit that delays the positive edge of a signal by one cycle.

Your Submission:

The due date for submitting this assignment has passed.
As per our records you have not submitted this assignment.