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NPTEL (https://swayam.gov.in/explorer?ncCode=NPTEL) » Architectural Design of Digital Integrated Circuits (course)

Announcements (announcements)

About the Course (https://swayam.gov.in/nd1_noc20_ee37/preview) Ask a Question (forum)

Progress (student/home) Mentor (student/mentor)

Due on 2020-04-17, 23:59 IST

1. A) Draw the circuit of a 4x1 mux using 2 input NAND gates only.
   B) Draw the circuit of a 4x1 mux using any input NAND gates.
2. Draw the Clock gated version for a 4-bit shift register. Consider a complex gate with internal structure as shown in figure below. One of the inputs gets clock while all others get data signals. What all (and what type of) clock gating checks exist?

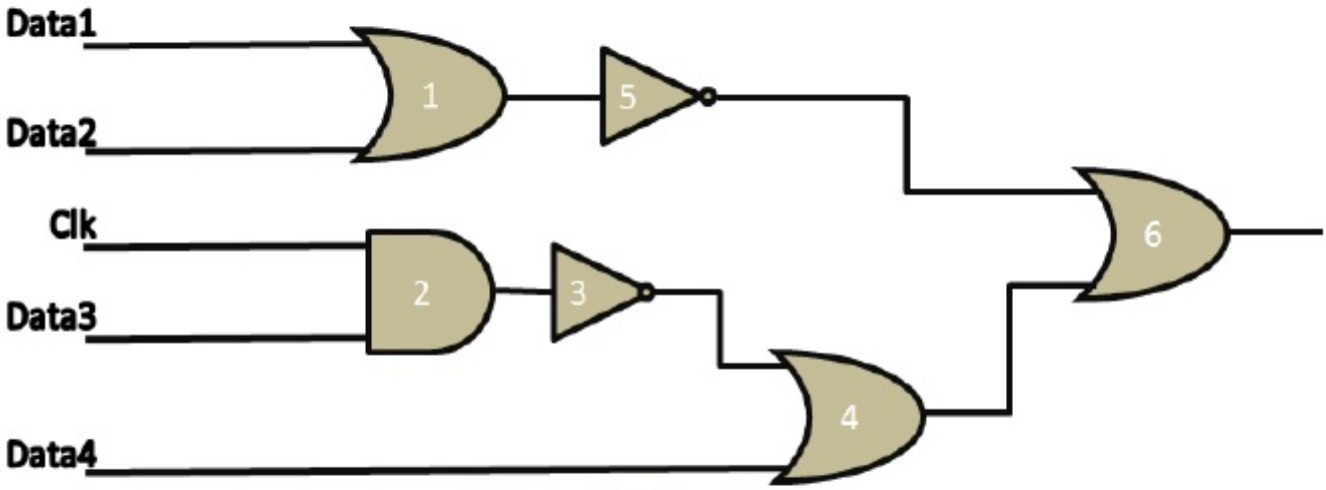

Figure:Problem figure

3. Implement 3 and 4 variable function using 8:1 MUX Implement 3 and 4 variable function using 8:1 MUX.
4. Explain the need for synchronizer in modern days VLSI circuit design? What type of synchronizers is mainly used VLSI circuit design. Draw the logic design of them with their working principle.
5. Why clock gating checks are needed? Explain clock gating checks for a multiplexer.

Your Submission:

The due date for submitting this assignment has passed.
As per our records you have not submitted this assignment.