Due on 2020-04-10, 23:59 IST

1. Figure below shows a timing path from a positive edge-triggered flip-flop to a positive edge-triggered flip-flop. Considering clock frequency of 200 MHz, find the setup and hold slacks for this timing path.

![Timing Path 1](image1)

2. Figure below shows a timing path from a positive edge-triggered flip-flop to a positive edge-triggered flip-flop. Considering ideal clocks, and clock frequency of 100 MHz, find the setup and hold slacks for this timing path.

![Timing Path 2](image2)
3. Which type of jitter matters for timing slack calculation? What will happen to clock jitter if I divide down the clock? What will happen to clock jitter for a multicycle path?

4. A) Can jitter in clock effect setup and hold violations? What is the difference between normal buffer and the clock buffer?  
   B) What is a glitch? How are glitches harmful?

5. A) What is time borrowing? Consider below figure, wherein minimum pulse width requirement of a flip-flop is 590 ps. It is getting clocked by a PLL of 500 MHz with a duty cycle variation of 60 ps. There are 30 buffers in clock path, each having a rise delay of 60 ps and fall delay of 48 ps. Will this setup be able to meet the duty cycle requirement of flip-flop? Find the slack available.

   ![](image)

   B) How is there degradation in duty cycle of clock? How duty cycle degradation impacts timing?

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Your Submission:

The due date for submitting this assignment has passed.
As per our records you have not submitted this assignment.