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NPTEL (https://swayam.gov.in/explorer?ncCode=NPTEL) » Architectural Design of Digital Integrated Circuits (course)

Announcements (announcements)

About the Course (https://swayam.gov.in/nd1_noc20_ee37/preview) Ask a Question (forum)

Progress (student/home) Mentor (student/mentor)

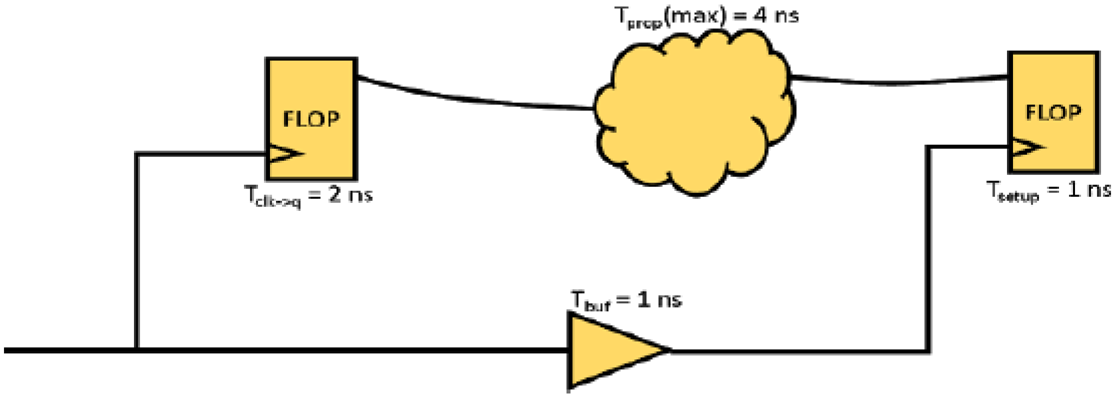
Due on 2020-04-03, 23:59 IST

1. A) Explain Positive, negative and zero setup time
   B) Explain Positive, negative and zero hold time

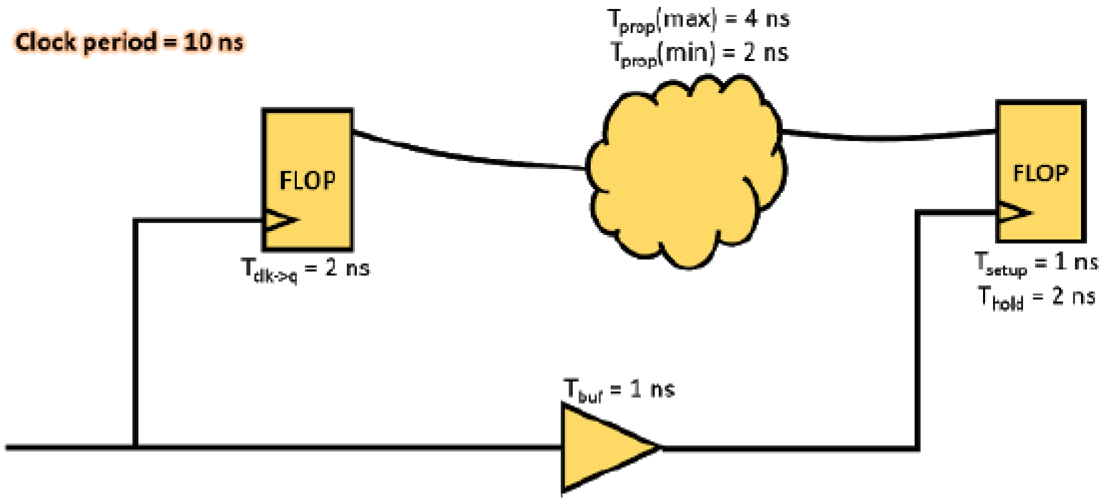
2. A) How positive edge trigger register to positive latch path is zero cycle. But positive latch to rising flop is full cycle?
   B) How can we generate a pulse for every edge of the incoming pulse?

3. How a latch/flip-flop goes metastable?

4. Figure below shows a timing path from a positive edge-triggered register to a positive edge-triggered register. Can you figure out the maximum frequency of operation for this path?



5. Figure below shows a timing path from positive edge-triggered register to a positive edge-triggered register. Can you figure out if there is any setup and/or hold violation in the following circuit?



Your Submission:

The due date for submitting this assignment has passed.
As per our records you have not submitted this assignment.