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NPTEL (<https://swayam.gov.in/explorer?ncCode=NPTEL>) » Architectural Design of Digital Integrated Circuits (course)

Announcements (announcements)

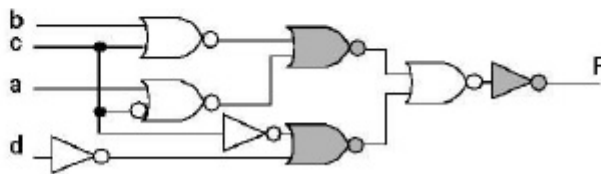
About the Course (https://swayam.gov.in/nd1_noc20_ee37/preview) Ask a Question (forum)

Progress (student/home) Mentor (student/mentor)

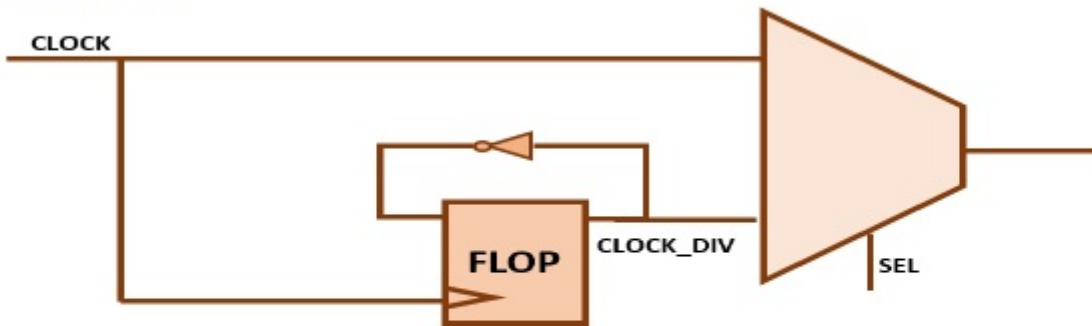
Due on 2020-03-27, 23:59 IST

1. Draw different circuits for implementing $(A+B+C+D+E+F+G+H)/8$. Analyze the accuracy in each of the case and find out the optimal circuit in respect of accuracy. Describe the advantages and disadvantages of each of the implementation
2. What is glitch in the digital circuit? Explain the glitch considering one example (with full waveform). How to reduce the glitch in the circuit.
3. Find all the hazards in F?

Find All The Hazards In F.



4. In the following figure, it is desired to toggle the select of the mux from CLOCK_DIV to CLOCK and both the clocks are running. What are the architectural and STA considerations for the same?



5. a) In Back-end Design Which Violation Has More Priority? Why?
 b) What Is Negative Slack? What Is Slack?
 c) How Can You Avoid Hold Time Violations? How Can You Avoid Setup Time Violations?

Your Submission:

The due date for submitting this assignment has passed.
 As per our records you have not submitted this assignment.

