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**NPTEL (<https://swayam.gov.in/explorer?ncCode=NPTEL>) » Architectural Design of Digital Integrated Circuits (course)**

Announcements ([announcements](#))

**About the Course ([https://swayam.gov.in/nd1\\_noc20\\_ee37/preview](https://swayam.gov.in/nd1_noc20_ee37/preview))** [Ask a Question \(forum\)](#)

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**Due on 2020-03-13, 23:59 IST**

1. Draw a circuit which can implement  $X * 2^n$ . Where x is of 16 bit and n is of 4 bit.
2. Describe how the pipelining and parallel processing helps in obtaining low power consumption in digital VLSI design.
3. Draw the architecture of a 3-bit conditional sum adder.
4. Draw the circuit which can compute sort 4 different numbers in ascending order.
5. Draw the circuit for finding out the square root of a given number.

## Your Submission:

The due date for submitting this assignment has passed.  
As per our records you have not submitted this assignment.

