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Due on 2020-03-06, 23:59 IST

1. Make a simple circuit whose output clock is four times higher in frequency to the input clock.
2. Make one digital circuit which takes a BCD digit as input and produces the output that is equal to 3 times of the input digit in the same format.
3. What is duty cycle? Explain in details how duty cycle impacts on timing analysis of any circuit design.
4. How can you implement one and gate using multiplexer? A 2-input multiplexer has both of its input getting value of 1. Will there be any toggle (glitch) happening at the output of the mux? If yes is it expected? What if both the inputs are getting value 0.
5. What is setup time and hold time? What is the cause of origin of setup and hold time? How do you check setup and hold time in a design? How to mitigate the setup and hold time violations?

Your Submission:

The due date for submitting this assignment has passed.
As per our records you have not submitted this assignment.