Draw the circuit which can compute minimum of 4 different numbers.

Let: Let A, B, C, D are four different numbers.

Now we can implement the circuit in two ways: Serial & Parallel.

Serial Architecture

Parallel Architecture

C<sub>2</sub>, C<sub>3</sub>

Comparator

M<sub>2</sub>; M<sub>3</sub>

2:1 MUX

C<sub>1</sub>, C<sub>2</sub>, C<sub>3</sub>

Comparator

M<sub>1</sub>, M<sub>2</sub>, M<sub>3</sub>

2:1 MUX
Question 2: Draw the circuit which can compute the maximum amongst 4 different numbers.

Solution:
Let the numbers are A, B, C, D.

**Serial Architecture**

**Parallel Architecture**
Derive the logical expressions for the 4-bit incrementer by 2 circuits and draw the architecture of it.

**Solu.** Let $A_1, A_2, A_3, A_4$ are 4-bits of the incrementer circuits.

Now, consider

\[
\begin{align*}
A_4 & \quad 0 \\
A_3 & \quad 0 \\
A_2 & \quad 0 \\
A_1 & \quad 0 \\
\end{align*}
\]

Now, consider

\[
\begin{align*}
S_1 &= A_1 \oplus 0 \oplus 0 = A_1 \\
C_1 &= (A_1 \cdot 0) + (0 \cdot 0) + (A_0 \cdot 0) = 0 \\
S_2 &= A_2 \oplus 1 \oplus 0 = A_2 \\
C_2 &= (A_2 \cdot 1) + (1 \cdot 0) + (A_1 \cdot 0) = A_2 \\
S_3 &= A_3 \oplus 0 \oplus A_2 = A_3 \oplus A_2 \\
C_3 &= (A_3 \cdot 0) + (A_2 \cdot 0) + (A_1 \cdot A_2) = A_3 A_2 \\
S_4 &= A_4 \oplus 0 \oplus A_3 A_2 = A_4 \oplus A_3 A_2 \\
C_{out} &= (A_4 \cdot 0) + (A_3 A_2 \cdot 0) + (A_4 \cdot A_3 A_2) \\
&= A_4 A_3 A_2
\end{align*}
\]

Here one of the input to the 4-bit adder is $A_3 A_2 A_4$, and another input is $0010$.

For a single FA cell, the

\[
\begin{align*}
\text{Sum} &= A_3 \oplus B \oplus C_{in} \\
\text{Carry} &= (A_3 \oplus B) + (B \oplus C_{in}) + (A_3 \oplus C_{in})
\end{align*}
\]
Now from the logical expressions we have got earlier, the architecture will be as shown below.

Derive the logical expressions for 4-bit decoder circuit by 2 and draw the architecture of it.

Sol. :— Let the 4-bits are $A_4, A_3, A_2, A_1$.

Now, as we have to do decrement by 2, we can do 2's complement addition instead.

Then, 2 can be represented as in 2's complement form:

$$2 = 0010 \xrightarrow{2\text{\text{^c}omplement}} 1110$$

Note,

4-bit decoder circuit diagram.
For FA1 \[ s_1 = A_1 \oplus 0 \oplus 0 = A_1 \]
\[ c_1 = (A_1 \cdot 0) + (0 \cdot 0) + (0 \cdot A_1) = 0 \]

For FA2 \[ s_2 = A_2 \oplus 1 \oplus 0 = A_2 \]
\[ c_2 = (A_2 \cdot 1) + (1 \cdot 0) + (A_2 \cdot 0) = A_2 \]

For FA3 \[ s_3 = A_3 \oplus 1 \oplus A_2 = A_3 \oplus A_2 \]
\[ c_3 = (A_3 \cdot 1) + (A_2 \cdot 1) + (A_3 \cdot A_2) = A_3 + A_2 \]

For FA4 \[ s_4 = A_4 \oplus 1 \oplus (A_3 + A_2) \]
\[ c_4 = (A_4 \cdot 1) + ((A_3 + A_2) \cdot 1) + (A_4 \cdot (A_3 + A_2)) = A_4 + A_3 + A_2 \]

Note based on these expressions the final architecture of the decrementer circuit will be:

![Diagram of decrementer circuit]
Draw the architecture of a controlled 1's complement/2's complement circuit.

**Step:** First draw the 1's complement circuit considering the enable signal.

\[
\overline{A_4} \quad \overline{A_3} \quad \overline{A_2} \quad \overline{A_1} \quad EN = 1
\]

Here \( \overline{A_m} = A_m \oplus E \)

For two's complement, we have to add 1 to the \( \{A_4, A_3, A_2, A_1\} \). If we consider the incrementer circuit by 1 logic then the carry logic can be written as

\[
C_i = A_i + C_{i-1}, \quad \text{where} \quad C_0 = 0, \quad \text{and} \quad i = 1, 2, 3, 4
\]

\[
S_i = A_i \oplus E \oplus C_{i-1}
\]

The architecture for controlled 1's comp/2's comp circuit will be:

[Diagram of the circuit]