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NPTEL (https://swayam.gov.in/explorer?ncCode=NPTEL) » Architectural Design of Digital Integrated Circuits (course)

Announcements (announcements)

About the Course (https://swayam.gov.in/nd1_noc20_ee37/preview) Ask a Question (forum)

Progress (student/home) Mentor (student/mentor)

Due on 2020-02-28, 23:59 IST

1. Draw the architecture (serial and parallel) of a circuit which can compute the minimum number amongst 4 different numbers.
2. Draw the architecture (serial and parallel) of a circuit which can compute the maximum number amongst 4 different numbers.
3. Derive the logical expression for one 5-bit incrementer circuits which can increment at every step by a factor of 2. Draw the architecture of the particular circuit.
4. Derive the logical expression for one 5-bit decrementer circuits which can increment at every step by a factor of 2. Draw the architecture of the particular circuit.
5. Draw the architecture of one controlled 1’s complement and 2’s complement circuit.

Your Submission:

The due date for submitting this assignment has passed.
As per our records you have not submitted this assignment.