Assignment on Architectural Design of Digital Integrated Circuits

Number-3

(Each of the questions carries 1 mark each)

1. How many inputs will a decimal-to-BCD encoder have?
   a) 4
   b) 8
   c) 10
   d) 16
   Answer: c
   Explanation: Decimal-to-bcd converter decimal values are inputs which range from 0-9. So, total ten inputs a decimal-to-BCD encoder has

2. How is an encoder different from a decoder?
   a) The output of an encoder is a binary code for 1-of-N input
   b) The output of a decoder is a binary code for 1-of-N input
   c) The output of an encoder is a binary code for N-of-1 output
   d) The output of an decoder is a binary code for N-of-1 output
   Answer: a
   Explanation: An encoder different from a decoder because of the output of an encoder is a binary code for 1-of-N input.

3. If we record any music in any recorder, such types of process is called
   a) Multiplexing
   b) Encoding
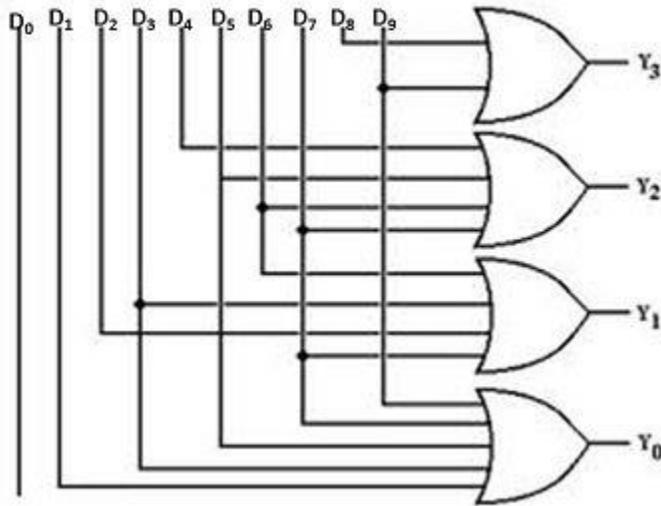   c) Decoding
   d) None of the Mentioned
   Answer: b
   Explanation: If we record any music in any recorder, it means that we are giving data to a recorder. So, such process is called encoding

4. How many OR gates are required for a Decimal-to-bcd encoder?
   a) 2
   b) 10
   c) 3
   d) 4

Answer: d

Explanation: This is clear from the diagram that it requires 4 OR gates:

5. For 8-bit input encoder how many combinations are possible?

   a) 8

   b) 2^8

   c) 4

   d) 2^4

   Answer: b

   Explanation: There are 2^8 combinations are possible for a 8-bit input encoder but out of which only 8 are used using 3 output lines. It is a disadvantage of encoder.

6. Can an encoder be called as multiplexer?

   a) No

   b) Yes

   c) Sometimes

   d) Never

   Answer: b

   Explanation: A multiplexer or MUX is a combination circuit that contains more than one input line, one output line and more than one selection line. Whereas, an encoder is also considered a type of multiplexer but without a single output line.

7. If two inputs are active on a priority encoder, which will be coded on the output?

   a) The higher value

   b) The lower value

   c) Neither of the inputs

   d) Both of the inputs

   Answer: a

   Explanation: If two inputs are active on a priority encoder, the input of higher value will be coded in the output

8. How many inputs are required for a 1-of-16 decoder?
   a) 2
   b) 16
   c) 8
   d) 4
   Answer: d
   Explanation: 'd' is correct because 1-of-10 stands for BCD to decimal decoder.
9. Which error detection method uses one's complement arithmetic?
   a) Simple parity check
   b) Two-dimensional parity check
   c) CRC
   d) Checksum
   Answer: d
   Explanation: A checksum can be generated simply by adding bits. Hence, one's complement arithmetic uses checksum
10. What is the maximum possible range of bit-count specifically in n-bit binary counter consisting of 'n' number of flip-flops?
    a) 0 to 2n
    b) 0 to 2n-1
    c) 0 to 2n+1
    d) 0 to 2n+1/2
    Answer: c
    Explanation: The maximum possible range of bit-count specifically in n-bit binary counter consisting of 'n' number of flip-flops is 0 to 2n+1.
11. Internal propagation delay of asynchronous counter is removed by
    a) Ripple counter
    b) Ring counter
    c) Modulus counter
    d) Synchronous counter
    Answer: d
    Explanation: Internal propagation delay of asynchronous counter is removed by synchronous counter because clock input is given to each flip-flop individually in synchronous counter.
12. The terminal count of a typical modulus-10 binary counter is
    a) 0000
    b) 1010
    c) 1001
    d) 1111
    Answer: c
    Explanation: Modulus-10 means count from 0 to 9. So, terminal count is 9 (1001).

13. A 5-bit asynchronous binary counter is made up of five flip-flops, each with a 12 ns propagation delay. The total propagation delay (tp(total)) is
    a) 12 ms
    b) 24 ns
    c) 48 ns
    d) 60 ns
    Answer: d
    Explanation: Each bit has propagation delay = 12ns. So, 5 bits = 12ns * 5 = 60ns.
14. An asynchronous 4-bit binary down counter changes from count 2 to count 3. How many transitional states are required?
    a) 1
    b) 2
    c) 8
    d) 15
    Answer: d
    Explanation: Transitional state is given by $2^4 - 1 = 15$. So, total transitional states are 15.
15. A down counter using n-flip-flops count
    a) Downward from a maximum count
    b) Upward from a minimum count
    c) Downward from a minimum to maximum count
    d) None of the Mentioned
    Answer: a
    Explanation: As the name suggests down counter means counting occurs from a higher value to lower value (i.e. (2^n – 1) to 0).
16. A ripple counter's speed is limited by the propagation delay of:
    a) Each flip-flop
    b) All flip-flops and gates
    c) The flip-flops only with gates
    d) Only circuit gates
    Answer: a
    Explanation: A ripple counter is something that is derived by other flip-flops. Its like a series of Flip Flops. Output of one FF becomes the input of the next. Because ripple counter is composed of FF only and no gates are there other than FF, so only propagation delay of FF will be taken into account.
17. A bidirectional 4-bit shift register is storing the nibble 1110. Its input is LOW. The nibble 0111 is waiting to be entered on the serial data-input line. After two clock pulses, the shift register is storing _____
    a) 1110
    b) 0111

c) 1000

d) 1001

Answer: d

Explanation: Stored nibble | waiting nibble

0111 | 1110, Initially

111 | 1100, 1st pulse

11 | 1001, 2nd pulse

18. In a parallel in/parallel out shift register, D0 = 1, D1 = 1, D2 = 1, and D3 = 0. After three clock pulses, the data outputs are _____

a) 1110

b) 0001

c) 1100

d) 1000

Answer: b

Explanation: Parallel in parallel out gives the same output as input.

19. The group of bits 10110111 is serially shifted (right-most bit first) into an 8-bit parallel output shift register with an initial state 11110000. After two clock pulses, the register contains

a) 10111000

b) 10110111

c) 11110000

d) 11111100

Answer: d

Explanation: It can be solved as per the explanation given for question number 3.

20. By adding recirculating lines to a 4-bit parallel-in serial-out shift register, it becomes a _____, _____, and _____out register.

a) Parallel-in, serial, parallel

b) Serial-in, parallel, serial

c) Series-parallel-in, series, parallel

d) Bidirectional in, parallel, series

Answer: a

Explanation: One bit shifting takes place just after the output obtained on every register. Hence, by adding recirculating lines to a 4-bit parallel-in serial-out shift register, it becomes a Parallel-in, Serial, and Parallel-out register.

21. The full form of HDL is

a) Higher Descriptive Language

b) Higher Definition Language

c) High Definition Language

d) High Descriptive Language

Answer: c

Explanation: The full form of HDL is 'Higher Definition Language'

22. The full form of VHDL is

a) Very High Descriptive Language

b) Very High Definition Language

c) Variable Definition Language

d) None of the Mentioned

Answer: b

Explanation: The full form of VHDL is 'Very High Definition Language'.

23. Which design activity helps in the transformation of the floating point arithmetic to a fixed point arithmetic?

a) high-level transformation

b) scheduling

c) compilation

d) task-level concurrency management

Answer: a

Explanation: The high-level transformation are responsible for the high optimizing transformations, that is, for the loop interchanging and the transformation of the floating point arithmetic to the fixed point arithmetic can be done by the high-level transformation

24. Speed power product is measured as the product of

a) gate switching delay and gate power dissipation

b) gate switching delay and gate power absorption

c) gate switching delay and net gate power

d) gate power dissipation and absorption

Answer: a

Explanation: Speed power product is measure in picojoules and it is the product of gate switching delay and gate power dissipation.

25. _____ is used to deal with effect of process, voltage and temperature variation

a) chip level technique

b) logic level technique

c) switch level technique

d) system level technique

Answer: d

Explanation: Designers must simulate multiple fabrication process or use system level technique for dealing with effects of variation.

26. _____ architecture is used to design VLSI

a) system on a device

b) single open circuit

c) system on a chip

d) system on a circuit

Answer: c

Explanation: SoC that is system on a chip architecture is used to design the very high level integrated circuit.

27. The design flow of VLSI system is

1. architecture design 2. market requirement 3. logic design 4. HDL coding

a) 2-1-3-4

b) 4-1-3-2

c) 3-2-1-4

d) 1-2-3-4

Answer: a

Explanation: The order of the design flow of VLSI circuit is market requirement, architecture design, logic design, HDL coding and then verification.

28. _____ is used in logic design of VLSI

a) LIFO

b) FIFO

c) FILO

d) LILO

Answer: b

Explanation: First in first out (FIFO) technique and finite state machine technique is used in the logic design of the VLSI circuits.

29. Physical and electrical specification is given in

a) architectural design

b) logic design

c) system design

d) functional design

Answer: d

Explanation: Functional design defines the major functional units of the system, interconnections, physical and electrical specifications.

30. Which is the high level representation of VLSI design

a) problem statement

b) logic design

c) HDL program

d) functional design

Answer: a

Explanation: Problem statement is a high level representation of the system. Performance, functionality and physical dimensions are considered here.

31. Gate minimization technique is used to simplify the logic.

a) true

b) false

Answer: a

Explanation: Gate minimization technique is used to find the simplest, smallest and effective implementation of the logic.

32. In clocked CMOS logic, output in evaluated in
    a) on period
    b) off period
    c) both periods
    d) half of on period

    Answer: a

    Explanation: In clocked CMOS logic, the logic is evaluated only in the on period of the clock. And owing to the extra transistor in series, slower rise time and fall times are expected.

33. In clocked CMOS logic, rise time and fall time are
    a) faster
    b) slower
    c) faster first and then slows down
    d) slower first and then speeds up

    Answer: b

    Explanation: In clocked CMOS logic, rise time and fall time are slower because of more number of transistors in series.

34. Which are easier to design?
    a) clocked circuits
    b) asynchronous sequential circuits
    c) clocked circuits with buffer
    d) asynchronous sequential circuits with buffers

    Answer: a

    Explanation: Clocked circuitry are easier to design than the asynchronous sequential circuits. But it is slower than the asynchronous sequential circuit.

35. In which design all circuitry and all interconnections are designed?
    a) full custom design
    b) semi-custom design
    c) gate array design
    d) transistor design

    Answer: a

    Explanation: Full custom design is the complete design for the implementation. It contains all circuitry and all interconnenctions/communication paths

36. In which method regularity is used to reduce complexity?
    a) random approach
    b) hierarchical approach

c) algorithmic approach

d) semi-design approach

Answer: b

Explanation: Hierarchical approach is in the one in which principles of iteration or regularity can be used to reduce the complexity of the design task.

37. Which design is faster?

a) full custom design

b) semi-custom design

c) gate array design

d) transistor design

Answer: c

Explanation: Gate array design is faster than a prototype full-custom design and the final custom designs must be carefully optimized

38. Which has relatively low-level capabilities?

a) hand-crafted designs

b) computer assisted textual entry

c) computer assisted graphical entry

d) silicon compiler-based design

Answer: b

Explanation: Computer-assisted textual entry has programs which may be relatively low-level capabilities and it allows the entry of rectangular boxes, wires etc

39. Which method uses high level programming language?

a) hand-crafted designs

b) computer assisted textual entry

c) computer assisted graphical entry

d) silicon compiler-based design

Answer: d

Explanation: Silicon compiler-based design uses high level approach and uses special languages like high level language compilers.

40. Which method uses reduced number of partial products?

a) baugh-wooley algorithm

b) wallace trees

c) dadda multipliers

d) modified booth encoding

Answer: d

Explanation: Multiplication in multipliers is done by obtaining partial products and then summing it up. Modified booth encoding reduces the number of partial products that must be summed.

41. Which multiplier is very well suited for twos complement numebers?

a) baugh-wooley algorithm

b) wallace trees

c) dadda multipliers

d) modified booth encoding

Answer: a

Explanation: Baugh-wooley method is used to design multipliers that are regular in structure and is very well suited for twos complement numbers.

42. Which method reduces number of cycles of operation?

a) baugh-wooley algorithm

b) wallace trees

c) dadda multipliers

d) modified booth encoding

Answer: d

Explanation: Modified booth encoding algorithm avoids many idle cells in a cellular multiplier as well as reduces the number of cycles compared with the serial-parallel multiplier.

43. The completion time for multiplication time in baugh-wooley method is

a) n

b) 2n

c) 3n

d) 4n

Answer: b

Explanation: The completion time for multiplication in Braun or Baugh-wooley is proportional to 2n where as completion time in Wallace tree method is proportional to log(base 2)(n).

44. In which method minimum number of adder cells are used?

a) baugh-wooley algorithm

b) wallace trees

c) dadda multipliers

d) modified booth encoding

Answer: c

Explanation: Dadda multipliers are similar to Wallace trees but it has reduced number of adder cells. This is a technique developed from Wallace tree but with an improvement.

45. Which method is suitable for larger operands?

a) baugh-wooley algorithm

b) wallace trees

c) dadda multipliers

d) modified booth encoding

Answer: b

Explanation: Wallace tree multipliers should be used for larger operands and where the performance is critical.

46. A sequential circuit contains combinational logic and storage elements in
    a) feedback path
    b) output node
    c) input node
    d) non feedback path
    Answer: a
    Explanation: A sequential circuit contains combinational logic and storage elements in feedback path.
47. To minimize the design effort, regularity should be
    a) low
    b) high
    c) very low
    d) very high
    Answer: b
    Explanation: Regularity is a qualitatie parameter and it should be high as possible to minimize the design effort required for any system
48. In the adder, sum is stored in
    a) series
    b) cascade
    c) parallel
    d) registers
    Answer: c
    Explanation: The sum is stored in parallel at the output of the adder from where it may be fed through the shifter and back to the register array.
49. For carry skip adder, the minimum total propogation delay can be obtained when m is
    a) sqrt (nk1/k2)
    b) sqrt (2nk1/k2)
    c) sqrt (2k1/nk2)
    d) sqrt (nk1k2/2)
    Answer: b
    Explanation: For carry skip adder the total propogation delay T is given by 2((n/M)-1)k1 + (M-2)k2. The minimum value of T can be obtained when m is sqrt(2nk1/k2).
50. Inverters are essential for
    a) NAND gates
    b) NOR gates
    c) sequential circuits
    d) all of the mentioned
    Answer: d
    Explanation: Inverters are needed for restoring logic levels for NAND and NOR gates, sequential and memory circuits.