Architectural Design on Digital ICS

Assignment-2

1. In 2's complement representation the number 11100101 represents the decimal number ……
   A. +37
   B. -31
   C. +27
   D. -27

Answer: D

2. A decade counter skips ……..
   A. binary states 1000 to 1111
   B. binary states 0000 to 0011
   C. binary states 1010 to 1111
   D. binary states 1111 to higher

Answer: C

3. BCD input 1000 is fed to a 7 segment display through a BCD to 7 segment decoder/driver. The segments which will lit up are …….
   A. *a, b, d*
   B. *a, b, c*
   C. all
   D. *a, b, g, c, d*

Answer: C

4. A ring counter with 5 flip flops will have ……. states.
   A. 5
   B. 10
   C. 32
   D. Infinite

Answer: A

5. In the expression A + BC, the total number of minterms will be ……

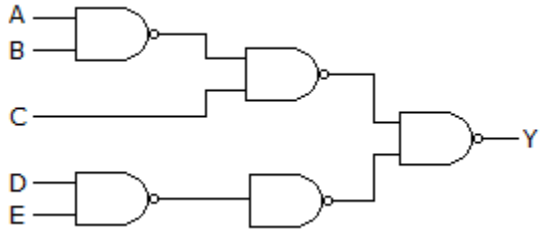
A. 2
B. 3
C. 4
D. 5

Answer: D

6. Decimal 43 in hexadecimal and BCD number system is respectively……. and ……..
   A. B2 and 01000011
   B. 2B and 01000011
   C. 2B and 00110100
   D. B2 and 01000100

Answer: B

7. The circuit of the given figure realizes the function ……



1. $Y = (\overline{A} + \overline{B})\,C + \overline{DE}$
2. $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E}$
3. $AB + C + DE$
4. $AB + C(D + E)$

Answer: 1

8. A JK flip flop has t_{pd}= 12 ns. The largest modulus of a ripple counter using these flip flops and operating at 10 MHz is ……..
   A. 16
   B. 64
   C. 128
   D. 256

Answer: D
Explanation:

Number of flip-flops = $\frac{1}{12 \times 10^{-9} \times 10 \times 10^{6}} = \frac{1000}{120} = 8.333$ say 8

Modulus = $2^8 = 256$.

9. In a ripple counter,
   A. whenever a flipflop sets to 1, the next higher FF toggles
   B. whenever a flipflop sets to 0, the next higher FF remains unchanged
   C. whenever a flipflop sets to 1, the next higher FF faces race condition
   D. whenever a flipflop sets to 0, the next higher FF faces race condition

Answer: A
Explanation: In a ripple counter the effect ripples through the counter.

10. For the truth table of the given figure Y = …….

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

   A. A + B + C
   B. $\bar{A}$ +BC
   C. $\bar{A}$
   D. $\bar{B}$

Answer: D
Explanation:

$$Y = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,C + A\overline{B}\,\overline{C} + A\,\overline{B}\,C = \overline{A}\,\overline{B}\,(\overline{C} + C) + A\,\overline{B}\,(\overline{C} + C) = \overline{A}\,\overline{B} + A\overline{B} = \overline{B}(A + A) = \overline{B}.$$

11. A full adder can be made out of ……
   A. two half adders
   B. two half adders and a OR gate
   C. two half adders and a NOT gate
   D. three half adders

Answer: B

12. If the functions *w*, *x*, *y*, *z* are as follows

$w = R + \overline{P}Q + \overline{R}S$,

$x = PQ\overline{R}\,\overline{S} + PQ\overline{R}\,\overline{S} + P\overline{Q}\,\overline{R}\,\overline{S}$

$y = RS + \overline{PR + P\overline{Q} + \overline{P}\overline{Q}}$

$z = R + S + \overline{PQ + \overline{P}\overline{Q} \cdot \overline{R} + P\overline{Q} \cdot \overline{S}}$

A. w = z x = z
B. w = z, x = y
C. w = y
D. w = y = z

Answer: A

13. Minimum number of 2-input NAND gates required to implement the function F = (x + y) (Z + W) is ……..
    A. 3
    B. 4
    C. 5
    D. 6

Answer: B

Explanation:

$F = (\overline{x} + \overline{y})\,(z + w) = \overline{xy}.(z + w)$

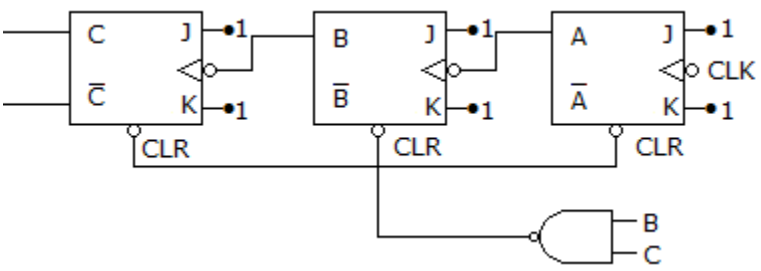
$= \overline{xy}z + \overline{xy}w$

$= \overline{\overline{F}} = \overline{\overline{\overline{xy}z + \overline{xy}\,w}} = \overline{\overline{\overline{xy}z} \cdot \overline{\overline{xy}\,w}}$ minimum no. of 2 input NAND gate.

14. A carry look ahead adder is frequently used for addition because
    A. it costs less
    B. it is faster
    C. it is more accurate
    D. uses fewer gates

Answer: B

15. The counter in the given figure is …….



A. Mod 3
B. Mod 6
C. Mod 8
D. Mod 7

Answer: B
Explanation: When counter is 110 the counter resets. Hence mod 6.

16. In register index addressing mode the effective address is given by ……..
    A. index register value
    B. sum of the index register value and the operand
    C. operand
    D. difference of the index register value and the operand

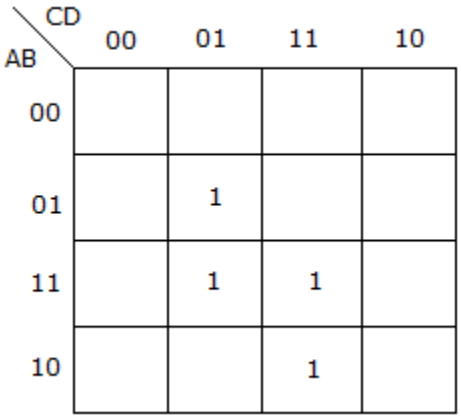
Answer: B
Explanation:
$4 = 2^2$, in up scaling digit will be shifted by two bit in right direction.

17. For the minterm designation Y = ∑ m (1, 3, 5, 7) the complete expression is ……..

1. $Y = \overline{A}\,\overline{B}C + A\,\overline{B}\,C$
2. $Y = \overline{A}\,\overline{B}\,C + A\,\overline{B}\,C + ABC + \overline{A}\,BC$
3. $Y = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,C + \overline{A}BC + A\,\overline{B}C$
4. $Y = \overline{A}\,\overline{B}\,\overline{C} + ABC + \overline{A}\,\overline{B}C + A\,\overline{B}C$

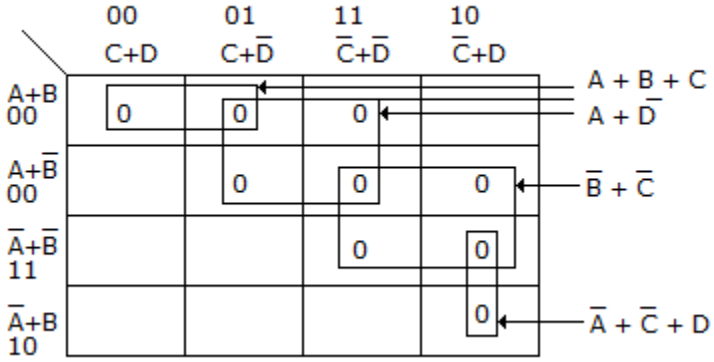
Answer : 2
Explanation:
Decimal number 1 = binary number 001 = $\overline{A}\,\overline{B}C$ Decimal number 7 = binary number 111= ABC,
Decimal number 3 = binary number 011= $\overline{A}BC$ Decimal number 5 = binary number 101= $A\overline{B}C$.
Hence result.

18. For the K map in the given figure the simplified Boolean expression is ……



1. $\overline{A}\,\overline{C} + \overline{A}\,\overline{D} + ABC$
2. $\overline{A}\,C + \overline{A}\,\overline{D} + ABC$
3. $\overline{A}\,C + \overline{A}\,\overline{D} + ACD$
4. $\overline{A}\,\overline{C} + \overline{A}\,\overline{D} + AB\,\overline{C}$

Answer : 1
Explanation:



19. A memory system of size 16 k bytes is to be designed using memory chips which have 12 address lines and 4 data lines each. The number of such chips required to design the memory system is …….
    A. 2
    B. 4
    C. 8
    D. 18

Answer : C
Explanation:
(16×1024×8)/(4096×4) = 8

20. In a BCD to 7 segment decoder the minimum and maximum number of outputs active at any time is ….
    A. 2 and 7
    B. 3 and 7
    C. 1 and 6
    D. 3 and 6

Answer: A
Explanation:
Minimum number of outputs when input is decimal 1 and maximum number of outputs when input is decimal 8.

21. 2’s complement of 11001011 is _____
    a) 01010111
    b) 11010100
    c) 00110101
    d) 11100010

Answer: c
Explanation: 2’s complement of a binary number is obtained by finding the 1’s complement of the number and then adding 1 to it.
2’s complement of 11001011 = 00110100 + 1 = 00110101.

22. On subtracting (01010)2 from (11110)2 using 1’s complement, we get _____
    a) 01001
    b) 11010
    c) 10101
    d) 10100

Answer: d
Explanation: Steps For Subtraction using 1’s complement are:
-> 1’s complement of the subtrahend is determined and added to the minuend.
-> If the result has a carry, then it is dropped and 1 is added to the last bit of the result.
-> Else, if there is no carry, then 1’s complement of the result is found out and a ‘-’ sign preceeds the result.

```
                    1 1 1
      Minuend -     1 1 1 1 0
1’s complement of subtrahend -  1 0 1 0 1
                  _____________
   Carry over -  1   1 0 0 1 1
                       1
                  _____________
```

1 0 1 0 0

23. On subtracting (010110)2 from (1011001)2 using 2's complement, we get _____
    a) 0111001
    b) 1100101
    c) 0110110
    d) 1000011

Answer: d
Explanation: Steps For Subtraction using 2's complement are:
-> 2's complement of the subtrahend is determined and added to the minuend.
-> If the result has a carry, then it is dropped and the result is positive.
-> Else, if there is no carry, then 2's complement of the result is found out and a '-' sign preceeds the result.

1's complement of subtrahend - 1 1 0 1 0 0 1

1 1 1

Minuend - 1 0 1 1 0 0 1

2's complement of subtrahend - 1 1 0 1 0 1 0

Carry over - 1 1 0 0 0 0 1 1

24. On addition of +38 and -20 using 2's complement, we get _____
    a) 11110001
    b) 100001110
    c) 010010
    d) 110101011

Answer: c
Explanation: Steps for Binary Addition Using 2's complement:
-> The 2's complement of the addend is found out and added to the first number.
-> The result is the 2's complement of the sum obtained.

Augend - 0 1 0 0 1 1 0

2's Complement of Subtrahend: 1 1 0 1 1 0 0

1 0 0 1 0 0 1 0

Answer: 0 1 0 0 1 0

25. On addition of -33 and -40 using 2's complement, we get _____
    a) 1001110

b) -110101
c) 0110001
d) -1001001

Answer: d
Explanation: The BCD form is written of the two given numbers, in their signed form. After which, normal binary addition is performed.
Augend is -40 and Subtrahend is -33.

Augend - 1 0 1 0 0 0 0 1 .....(a)
2's Complement of Subtrahend: 1 1 0 1 1 0 0 1 .....(b)

Addiing (a) and (b): 1 0 1 0 0 1 0 0 0
Since, there is no carry, so answer will be negative
and 2's complement of the above result is determined.

1 0 0 1 0 0 0
\+ 1

1 0 0 1 0 0 1

Answer: -1001001

26. If the number of bits in the sum exceeds the number of bits in each added numbers, it results in _____
    a) Successor
    b) Overflow
    c) Underflow
    d) Predecessor

Answer: b
Explanation: If the number of bits in the sum exceeds the number of bits in each added numbers, it results in overflow and is also known as excess-one. In case of any arithmetic operation, if the result has less number of bits than the operands, then it is known as underflow condition.

27. An overflow is a _____
    a) Hardware problem
    b) Software problem
    c) User input problem
    d) Input Output Error

Answer: b
Explanation: An overflow is a software problem which occurs when the processor cannot handle the result properly when it produces an out of the range output.

28. Logic circuitry is used to detect _____
    a) Underflow
    b) MSD
    c) Overflow
    d) LSD

Answer: c
Explanation: To check the overflow logic circuitry is used in each case. Overflow occurs when the processor cannot handle the result properly when it produces an out of the range output.

29. The advantage of 2's complement system is that _____
    a) Only one arithmetic operation is required
    b) Two arithmetic operations are required
    c) No arithmetic operations are required
    d) Different Arithmetic operations are required

Answer: a
Explanation: The advantage of 2's complement is that only one arithmetic operation is required for 2's complement's operation and that is only addition. Just by adding a 1 bit to 1's complement, we get 2's complement.

30. Which one is used for logical manipulations?
    a) 2's complement
    b) 9's complement
    c) 1's complement
    d) 10's complement

Answer: c
Explanation: For logical manipulations 1's complement is used, as all logical operations take place with binary numbers.

31. For arithmetic operations only _____
    a) 1's complement is used
    b) 2's complement
    c) 10's complement
    d) 9's complement

Answer: b
Explanation: Only 2's complement is used for arithmetic operations, as it is more fast.

32. The addition of +19 and +43 results as _____ in 2's complement system.
    a) 11001010
    b) 101011010

c) 00101010
d) 0111110

Answer: d
Explanation: The decimal numbers are converted to their respective binary equivalent and then the binary addition rules are applied.

33. Carry out BCD subtraction for (68) – (61) using 10’s complement method.
    a) 00000111
    b) 01110000
    c) 100000111
    d) 011111000

Answer: a
Explanation: First the two numbers are converted into their respective BCD form using 8421 sequence. Then binary subtraction is carried out.

34. The decimal equivalent of the excess-3 number 110010100011.01110101 is _____
    a) 970.42
    b) 1253.75
    c) 861.75
    d) 1132.87

Answer: a
Explanation: The conversion of binary numbers into digits ‘1100’, ‘1010’, ‘0011’, ‘0111’ and ‘0101’ gives ’12’, ‘5’, ‘3’, ‘7’ and ‘5’ respectively. Hence, the decimal number is 970.42.

35. Which of the following gate is known as coincidence detector?
    a) AND gate
    b) OR gate
    c) NOR gate
    d) NAND gate

Answer: a
Explanation: AND gate is known as coincidence detector due to multiplicity behaviour, as it outputs 1 only when all the inputs are 1.

36. The number of full and half adders are required to add 16-bit number is _____
    a) 8 half adders, 8 full adders
    b) 1 half adders, 15 full adders
    c) 16 half adders, 0 full adders
    d) 4 half adders, 12 full adders

Answer: b
Explanation: Half adder has two inputs and two outputs whereas Full Adder has 3 inputs and 2 outputs. One half adder can add the least significant bit of the two numbers whereas full adders are required to add the remaining 15 bits as they all involve adding carries.

37. Odd parity of word can be conveniently tested by _____
    a) OR gate
    b) AND gate
    c) NAND gate
    d) XOR gate

Answer: d
Explanation: Odd parity of word can be conveniently tested by XOR gate, since, XOR outputs 1 only when the input has odd number of 1's.

38. The time required for a gate or inverter to change its state is called _____
    a) Rise time
    b) Decay time
    c) Propagation time
    d) Charging time

Answer: c
Explanation: The time required for a gate or inverter to change its state is called propagation time.

39. In boolean algebra, the OR operation is performed by which properties?
    a) Associative properties
    b) Commutative properties
    c) Distributive properties
    d) All of the Mentioned

Answer: d
Explanation: The expression for Associative property is given by A+(B+C) = (A+B)+C & A*(B*C) = (A*B)*C.
The expression for Commutative property is given by A+B = B+A & A*B = B*A.
The expression for Distributive property is given by A+BC=(A+B)(A+C) & A(B+C) = AB+AC.

40. The expression for Absorption law is given by _____
    a) A + AB = A
    b) A + AB = B
    c) AB + AA' = A
    d) A + B = B + A

Answer: a
Explanation: The expression for Absorption Law is given by: A+AB = A.
Proof: A + AB = A(1+B) = A (Since 1 + B = 1 as per 1's Property).

41. DeMorgan's theorem states that _____
    a) (AB)' = A' + B'
    b) (A + B)' = A' * B
    c) A' + B' = A'B'
    d) (AB)' = A' + B

Answer: a
Explanation: The DeMorgan's law states that (AB)' = A' + B' & (A + B)' = A' * B', as per the Dual Property.

42. Complement of the expression A'B + CD' is _____
    a) (A' + B)(C' + D)
    b) (A + B')(C' + D)
    c) (A' + B)(C' + D)
    d) (A + B')(C + D')

Answer: b
Explanation: (A'B + CD')' = (A'B)'(CD')' (By DeMorgan's Theorem) = (A" + B')(C' + D") (By DeMorgan's Theorem) = (A + B')(C' + D).

43. The boolean function A + BC is a reduced form of _____
    a) AB + BC
    b) (A + B)(A + C)
    c) A'B + AB'C
    d) (A + C)B

Answer: b
Explanation: (A + B)(A + C) = AA + AC + AB + BC = A + AC + AB + BC (By Commutative Property) = A(1 + C + B) + BC = A + BC (1 + B + C =1 By 1's Property).

44. The expression Y=AB+BC+AC shows the _____ operation.
    a) EX-OR
    b) SOP
    c) POS
    d) NOR

Answer: b
Explanation: The given expression has the operation product as well as the sum of that. So, it shows SOP operation. POS will be the product of sum terms.

45. A product term containing all K variables of the function in either complemented or uncomplemented form is called a _____
    a) Minterm
    b) Maxterm
    c) Midterm
    d) ∑ term

Answer: a
Explanation: A product term containing all K variables of the function in either complemented or uncomplemented form is called a minterm. A sum term containing all K variables of the function in either complemented or uncomplemented form is called a maxterm.

46. A variable on its own or in its complemented form is known as a _____
    a) Product Term
    b) Literal
    c) Sum Term
    d) Word

Answer: b
Explanation: A literal is a single logic variable or its complement. For example — X, Y, A', Z, X' etc.

47. Canonical form is a unique way of representing _____
    a) SOP
    b) Minterm
    c) Boolean Expressions
    d) POS

Answer: c
Explanation: Boolean Expressions are represented through canonical form. An example of canonical form is A'B'C' + AB'C + ABC'.

48. A Karnaugh map (K-map) is an abstract form of _____ diagram organized as a matrix of squares.
    a) Venn Diagram
    b) Cycle Diagram
    c) Block diagram
    d) Triangular Diagram

Answer: a
Explanation: A Karnaugh map (K-map) is an abstract form of Venn diagram organized as a matrix of squares, where each square represents a Maxterm or a Minterm.

49. The K-map based Boolean reduction is based on the following Unifying Theorem: A + A’ = 1.
    a) Impact
    b) Non Impact
    c) Force
    d) Complementarity

Answer: b
Explanation: The given expression A +A’ = 1 is based on non-impact unifying theorem.

50. The prime implicant which has at least one element that is not present in any other implicant is known as _____
    a) Essential Prime Implicant
    b) Implicant
    c) Complement
    d) Prime Complement

Answer: a
Explanation: Essential prime implicants are prime implicants that cover an output of the function that no combination of other prime implicants is able to cover.