Architectural Design of Digital Integrated Circuits

Assignment 1

Full Marks: 50

Section A (Each question carries 1 mark)

1. A serial subtractor can be obtained by converting the serial adder by using the _____
   a) 1's complement system
   b) 2's complement system
   c) 10's complement
   d) 9's complement

Answer: b
Explanation: A serial subtractor can be obtained by converting the serial adder by using the 2's complement system. 9's complement and 10's complement are used for decimal numbers while adders deal with binary numbers.

2. The hexadecimal number (4B)16 is transmitted as an 8-bit word in parallel. What is the time required for this transmission if the clock frequency is 2.25 MHz?
   a) 444 ns
   b) 444 s
   c) 3.55 s
   d) 3.55 ms

Answer: a
Explanation: Because the clock pulse of 4-bit transmits the data of 8-bit word in parallel mode and this transmission is done at 2.25 MHz frequency. We know that: f=1/t and we can find the time required for this transmission by the clock pulse.
Therefore, time = (1/2.25) = 0.4444 us = 444.44 ns ~ 444ns.

3. In most applications, transistor switches used in place of relays?
   a) They consume less power
   b) They are faster
   c) They are quieter and smaller
   d) All of the Mentioned

Answer: d
Explanation: Transistors are of less consuming power, faster, quieter, smaller and its implementation is too easy. So, in most applications transistor switches are more preferred. And also, transistors can be current-controlled or voltage-controlled depending on our choice.

4.

The decimal number system represents the decimal number in the form of _____
a) Hexadecimal
b) Binary coded
c) Octal
d) Decimal

Answer: b
Explanation: Binary-coded decimal (BCD) is a class of binary encodings of decimal numbers where each decimal digit is represented by a fixed number of bits, usually four or eight. Hexadecimal and Octal are number systems having base 16 and 8 respectively.

5. The output sum of two decimal digits can be represented in _____
   a) Gray Code
   b) Excess-3
   c) BCD
   d) Hexadecimal

Answer: c
Explanation: The output sum of two decimal digits can be represented in BCD(Binary-coded decimal). Binary-coded decimal (BCD) is a class of binary encodings of decimal numbers where each decimal digit is represented by a fixed number of bits, usually four or eight.

6. The addition of two decimal digits in BCD can be done through _____
   a) BCD adder
   b) Full adder
   c) Ripple carry adder
   d) Carry look ahead

Answer: a
Explanation: The addition of two decimal digits in BCD can be done through BCD adder. Every input inserted, in addition by the user converted into binary and then proceed for the addition. Whereas, Full Adder, Ripple Carry Adder and Carry Look Adder are for the addition of binary bits.

7. The simplified expression of full adder carry is _____
   a) c = xy+xz+yz
   b) c = xy+xz
   c) c = xy+yz
   d) c = x+y+z

Answer: a
Explanation: A full adder is a combinational circuit having 3 inputs and 2 outputs, namely SUM and CARRY. The simplified expression of full adder carry is c = xy+xz+yz.

8.

The number of logic gates and the way of their interconnections can be classified as _____

a) Logical network
b) System network
c) Circuit network
d) Gate network

Answer: a
Explanation: The number of different levels of logic gates is represented in a fashion which is known as a logical network.

9. One positive pulse with tw = 75 μs is applied to one of the inputs of an exclusive-OR circuit. A second positive pulse with tw = 15 μs is applied to the other input beginning 20 μs after the leading edge of the first pulse. Which statement describes the output's relation with the inputs?
   a) The exclusive-OR output is a 20 s pulse followed by a 40 s pulse, with a separation of 15 s between the pulses
   b) The exclusive-OR output is a 20 s pulse followed by a 15 s pulse, with a separation of 40 s between the pulses
   c) The exclusive-OR output is a 15 s pulse followed by a 40 s pulse
   d) The exclusive-OR output is a 20 s pulse followed by a 15 s pulse, followed by a 40 s pulse

Answer: d
Explanation: When both the input pulses are high or low X-OR output is low. But when one of the input is high and another is low or vice-versa, output is high. In this problem for the first 20uS one input is high and another is low. So, obviously output is a high. for next 15uS both the input is high so output is low and for remaining 40uS(75-20-15) first input is still high and second one is low so output is high.

10. The carry look ahead adder is based on the principle of looking at the lower order bits of _____ and _____ if a high order carry is generated.
    a) Addend, minuend
    b) Minuend, subtrahend
    c) Addend, minuend
    d) Augend, addend

Answer: d
Explanation: The carry look ahead adder is based on the principle of looking at the lower order bits of the augend and addend if a high order carry is generated. A carry look ahead adder is a type of adder which reduces the propagation delay.

11. In serial addition, the addition is carried out _____
    a) 3 bit per second
    b) Byte by byte
    c) Bit by bit
    d) All bits at the same time

Answer: c
Explanation: In serial addition, the addition is carried out bit by bit.

12. Which statement below best describes a Karnaugh map?
    a) It is simply a rearranged truth table
    b) The Karnaugh map eliminates the need for using NAND and NOR gates
    c) Variable complements can be eliminated by using Karnaugh maps
    d) A Karnaugh map can be used to replace Boolean rules

Answer: a
Explanation: K-map is simply a rearranged truth table. It is a pictorial representation of truth table having a specific number of cells or squares, where each cell represents a Maxterm or a Minterm.

13. Each "0" entry in a K-map square represents:
    a) A HIGH for each input truth table condition that produces a HIGH output
    b) A HIGH output on the truth table for all LOW input combinations
    c) A LOW output for all possible HIGH input conditions
    d) A DON'T CARE condition for all possible input truth table combinations

Answer: a
Explanation: Each "0" entry in a K-map square represents a LOW output for all possible HIGH input conditions. Thus, it represents a Maxterm.

14. Which of the following statements accurately represents the two BEST methods of logic circuit simplification?
    a) Actual circuit trial and error evaluation and waveform analysis
    b) Karnaugh mapping and circuit waveform analysis
    c) Boolean algebra and Karnaugh mapping
    d) Boolean algebra and actual circuit trial and error evaluation

Answer: c
Explanation: The two BEST methods of logic circuit simplification are Boolean algebra and Karnaugh mapping. Boolean Algebra uses the Laws of Boolean Algebra for minimization of Boolean expressions while Karnaugh Map is a pictorial representation and reduction of the Boolean expression.

15. Looping on a K-map always results in the elimination of _____
    a) Variables within the loop that appear only in their complemented form
    b) Variables that remain unchanged within the loop
    c) Variables within the loop that appear in both complemented and uncomplemented form
    d) Variables within the loop that appear only in their uncomplemented form

Answer: c
Explanation: Looping on a K-map always results in the elimination of variables within the loop that appear in both complemented and uncomplemented form.

16. The basic building blocks of the arithmetic unit in a digital computers are _____
    a) Subtractors
    b) Adders
    c) Multiplexer
    d) Comparator

Answer: b
Explanation: The basic building blocks of the arithmetic unit in a digital computers are adders. Since, a parallel adder is constructed with a number of full-adder circuits connected in cascade. By controlling the data inputs to the parallel adder, it is possible to obtain different types of arithmetic operations.

17. Procedure for the design of combinational circuits are:
    A. From the word description of the problem, identify the inputs and outputs and draw a block diagram.
    B. Draw the truth table such that it completely describes the operation of the circuit for different combinations of inputs.
    C. Simplify the switching expression(s) for the output(s).
    D. Implement the simplified expression using logic gates.
    E. Write down the switching expression(s) for the output(s).
    a) B, C, D, E, A
    b) A, D, E, B, C
    c) A, B, E, C, D
    d) B, A, E, C, D

Answer: c
Explanation: Combinational circuits are the ones which do not depend on previous inputs and depends only on the present values. The given arrangement in option c is the right sequence for the designing of the combinational circuits.

18. The design of an ALU is based on _____
    a) Sequential logic
    b) Combinational logic
    c) Multiplexing
    d) De-Multiplexing

Answer: b
Explanation: The design of an ALU is based on combinational logic. Because the unit has a regular pattern, it can be broken into identical stages connected in cascade through carries.

19. If the two numbers include a sign bit in the highest order position, the bit conditions of interest are the sign of the result, a zero indication and _____
    a) An underflow condition
    b) A neutral condition
    c) An overflow condition
    d) One indication

Answer: c
Explanation: If the two numbers include a sign bit in the highest order position, the bit conditions of interest are the sign of the result, a zero indication and an overflow condition.

20. If the two numbers include a sign bit in the highest order position, the bit conditions of interest are the sign of the result, a zero indication and _____
    a) An underflow condition
    b) A neutral condition
    c) An overflow condition
    d) One indication

Answer: c
Explanation: If the two numbers include a sign bit in the highest order position, the bit conditions of interest are the sign of the result, a zero indication and an overflow condition.

21. If the two numbers are unsigned, the bit conditions of interest are the _____ carry and a possible _____ result.
    a) Input, zero
    b) Output, one
    c) Input, one
    d) Output, zero

Answer: d
Explanation: If the two numbers are unsigned, the bit conditions of interest are the output carry and a possible zero result.

22. In a combinational circuit, the output at any time depends only on the _____ at that time.
    a) Voltage
    b) Intermediate values
    c) Input values
    d) Clock pulses

Answer: c
Explanation: In a combinational circuit, the output at any time depends only on the input values at that time and not on past or intermediate values.

23. In a sequential circuit, the output at any time depends only on the input values at that time.
    a) Past output values
    b) Intermediate values
    c) Both past output and present input
    d) Present input values

Answer: c
Explanation: In a sequential circuit, the output at any time depends on the present input values as well as past output values. It also depends on clock pulses depending on whether it’s synchronous or asynchronous sequential circuits.

24. Which of the following will give the sum of full adders as output?
    a) Three point major circuit
    b) Three bit parity checker
    c) Three bit comparator
    d) Three bit counter

Answer: d
Explanation: Counters are used for counting purposes in ascending or descending order. Three bit counter will give the sum of full adders as output.

25. Which of the following gate is known as coincidence detector?
    a) AND gate
    b) OR gate
    c) NOR gate
    d) NAND gate

Answer: a
Explanation: AND gate is known as coincidence detector due to multiplicity behaviour, as it outputs 1 only when all the inputs are 1

26. The time required for a gate or inverter to change its state is called _____
    a) Rise time
    b) Decay time
    c) Propagation time
    d) Charging time

Answer: c
Explanation: The time required for a gate or inverter to change its state is called propagation time.

27. Why is the fan-out of CMOS gates frequency dependent?
    a) Each CMOS input gate has a specific propagation time and this limits the number of different gates that can be connected to the output of a CMOS gate
    b) When the frequency reaches the critical value the gate will only be capable of delivering 70% of the normal output voltage and consequently the output power will be one-half of normal and this defines the upper operating frequency
    c) The higher number of gates attached to the output the more frequently they will have to be serviced thus reducing the frequency at which each will be serviced with an input signal
    d) The input gates of the FETs are predominantly capacitive and as the signal frequency increases the capacitive loading also increases thereby limiting the number of loads that may be attached to the output of the driving gate

Answer: d
Explanation: Fan out is the measure of maximum number of inputs that a single logic gate output can drive. Actually power dissipation in CMOS circuits depends on clock frequency. As the frequency increases Pd also increases so fan-out depends on frequency.

28. Logic circuits that are designated as buffers, drivers or buffers/drivers are designed to have:
    a) A greater current/voltage capability than an ordinary logic circuit
    b) Greater input current/voltage capability than an ordinary logic circuit
    c) A smaller output current/voltage capability than an ordinary logic
    d) Greater the input and output current/voltage capability than an ordinary logic circuit

Answer: a
Explanation: Buffer circuits are usually incorporated to isolate the input from the output. Logic circuits that are designated as buffers, drivers or buffer/drivers are designed to have a greater current/voltage capability than an ordinary logic circuit.

29. What is the static charge that can be stored by your body as you walk across a carpet?
    a) 300 volts
    b) 3000 volts
    c) 30000 volts
    d) Over 30000 volts

Answer: d
Explanation: When a person walks across a carpeted or tile floor electric charge builds up in the body due to the friction between shoes and floor material. If the friction static is greater the voltage potential develop in the body will be greater. You start act as a capacitor. This is called Electrostatic discharge. The potential static charge that can develop from walking on tile floors is greater than 15000 volts while carpeted floors can generate in excess of 30000 volts.

30. Which of the following statements apply to CMOS devices?
    a) The devices should not be inserted into circuits with the power on
    b) All tools, test equipment and metal workbenches should be tied to earth ground
    c) The devices should be stored and shipped in antistatic tubes or conductive foam
    d) All of the Mentioned

Answer: d
Explanation: For CMOS devices, all the mentioned statements are applicable. The devices should not be inserted into circuits with the power on. All tools, test equipment and metal workbenches should be tied to earth ground. Also, the devices should be stored and shipped in antistatic tubes or conductive foam.

31. LSI means _____ and refers to _____ gates per chip.
    a) Long Scale Integration, more than 10 upto 10000
    b) Large Scale Integration, more than 100 upto 5000
    c) Large Short Integration, less than 10 and greater than 5000
    d) Long Short Integration, more than 10 upto 10000

    Answer: b
    Explanation: The full form of LSI is Large Scale Integration and refers to more than 100 upto 5000 gates per chip.

32. The full form of DIP is _____
    a) Dual-in-Long Package
    b) Dual-in-Line Package
    c) Double Integrated Package
    d) Double-in-Line Package

Answer: b
Explanation: The full form of DIP is Dual-in-Line Package.

Section B (Each question carries 3 mark)

1. **Given Only Two Xor Gates One Must Function As Buffer And Another As Inverter?**

Answer:

- Tie one of xor gates input to 1 it will act as inverter.
- Tie one of xor gates input to 0 it will act as buffer.

2. **What Is Difference Between Latch And Flip-flop?**

Answer: The main difference between latch and FF is that latches are level sensitive while FF is edge sensitive. They both require the use of clock signal and are used in sequential logic. For a latch, the output tracks the input when the clock signal is high, so as long as the clock is logic 1, the output can change if the input also changes. FF on the other hand, will store the input only when there is a rising/falling edge of the clock.

3. **Difference Between Mealy And Moore State Machine?**

Answer: Mealy and Moore models are the basic models of state machines. A state machine which uses only Entry Actions, so that its output depends on the state, is called a Moore model. A state machine which uses only Input Actions, so that the output depends on the state and also on inputs, is called a Mealy model. The models selected will influence a design but there are no general indications as to which model is better. Choice of a model depends on the application, execution means (for instance, hardware systems are usually best realized as Moore models) and personal preferences of a designer or programmer

Mealy machine has outputs that depend on the state and input (thus, the FSM has the output written on edges) Moore machine has outputs that depend on state only (thus, the FSM has the output written in the state itself.

Adv and Disadv
In Mealy as the output variable is a function both input and state, changes of state of the state variables will be delayed with respect to changes of signal level in the input variables, there are possibilities of glitches appearing in the output variables. Moore overcomes glitches as output dependent on only states and not the input signal level.

All of the concepts can be applied to Moore model state machines because any Moore state machine can be implemented as a Mealy state machine, although the converse is not true.
Moore machine: the outputs are properties of states themselves…
which means that you get the output after the machine reaches a particular state, or to get some output your machine has to be taken to a state which provides you the output.The outputs are held until you go to some other state Mealy machine:
Mealy machines give you outputs instantly, that is immediately upon receiving input, but the output is not held after that clock cycle.

4. **How to Implement An And Gate Using Mux?**

Answer: This is the basic question that many interviewers ask. for and gate, give one input as select line, incase if u r giving b as select line, connect one input to logic '0' and other input to a.

5. **Compare And Contrast Synchronous And Asynchronous Reset?**

Answer: Synchronous reset logic will synthesize to smaller flip-flops, particularly if the reset is gated with the logic generating the d-input. But in such a case, the combinational logic gate count grows, so the overall gate count savings may not be that significant. The clock works as a filter for small reset glitches; however, if these glitches occur near the active clock edge, the Flip-flop could go metastable. In some designs, the reset must be generated by a set of internal conditions. A synchronous reset is recommended for these types of designs because it will filter the logic equation glitches between clock.
Problem with synchronous resets is that the synthesis tool cannot easily distinguish the reset signal from any other data signal. Synchronous resets may need a pulse stretcher to guarantee a reset pulse width wide enough to ensure reset is present during an active edge of the clock, if you have a gated clock to save power, the clock may be disabled coincident with the assertion of reset. Only an asynchronous reset will work in this situation, as the reset might be removed prior to the resumption of the clock. Designs that are pushing the limit for data path timing, can not afford to have added gates and additional net delays in the data path due to logic inserted to handle synchronous resets.
Asynchronous reset: The major problem with asynchronous resets is the reset release, also called reset removal. Using an asynchronous reset, the designer is guaranteed not to have the reset added to the data path. Another advantage favoring asynchronous resets is that the circuit can be reset with or without a clock present. Ensure that the release of the reset can occur within one clock period else if the release of the reset occurred on or near a clock edge then flip-flops may go into metastable state.

6. **What Is A Johnson Counter?**

Answer: Johnson counter connects the complement of the output of the last shift register to its input and circulates a stream of ones followed by zeros around the ring. For example, in a 4-register counter, the repeating pattern is: 0000, 1000, 1100, 1110, 1111, 0111, 0011, 0001, so on.