Unit 4 - Week 1

Assignment 1

The due date for submitting this assignment has passed. Due on 2020-02-12, 23:59 IST. As per our records you have not submitted this assignment.

1) 1 point
A serial subtractor can be obtained by converting the serial adder by using the ____________
   a) 1's complement system
   b) 2's complement system
   c) 10's complement
   d) 9's complement

   No, the answer is incorrect.
   Score: 0
   Accepted Answers:
   b)

2) 1 point
The hexadecimal number (4B)16 is transmitted as an 8-bit word in parallel. What is the time required for this transmission if the clock frequency is 2.25 MHz?
   a) 444 ns
   b) 444 s
   c) 3.55 s
   d) 3.55 ms
3) In most applications, transistor switches used in place of relays?
   a) They consume less power
   b) They are faster
   c) They are quieter and smaller
   d) All of the Mentioned

No, the answer is incorrect.
Score: 0
Accepted Answers:
a)

4) The decimal number system represents the decimal number in the form of ____________
   a) Hexadecimal
   b) Binary coded
   c) Octal
   d) Decimal

No, the answer is incorrect.
Score: 0
Accepted Answers:
b)

5) The output sum of two decimal digits can be represented in ____________
   a) Gray Code
   b) Excess-3
   c) BCD
   d) Hexadecimal

No, the answer is incorrect.
Score: 0
Solutions

6) The addition of two decimal digits in BCD can be done through __________
   a) BCD adder
   b) Full adder
   c) Ripple carry adder
   d) Carry look ahead

   Accepted Answers:
   c) 1 point

   No, the answer is incorrect.
   Score: 0
   Accepted Answers:
   a)

7) The simplified expression of full adder carry is __________
   a) c = xy+xz+yz
   b) c = xy+xz
   c) c = xy+yz
   d) c = x+y+z

   Accepted Answers:
   d) 1 point

   No, the answer is incorrect.
   Score: 0
   Accepted Answers:
   a)

8) The number of logic gates and the way of their interconnections can be classified as __________
   a) Logical network
   b) System network
   c) Circuit network
   d) Gate network

   Accepted Answers:
   c) 1 point

   No, the answer is incorrect.
   Score: 0
   Accepted Answers:
   a)
One positive pulse with $t_w = 75 \mu s$ is applied to one of the inputs of an exclusive-OR circuit. A second positive pulse with $t_w = 15 \mu s$ is applied to the other input beginning 20 $\mu s$ after the leading edge of the first pulse. Which statement describes the output's relation with the inputs?

a) The exclusive-OR output is a 20 $\mu s$ pulse followed by a 40 $\mu s$ pulse, with a separation of 15 $\mu s$ between the pulses
b) The exclusive-OR output is a 20 $\mu s$ pulse followed by a 15 $\mu s$ pulse, with a separation of 40 $\mu s$ between the pulses
c) The exclusive-OR output is a 15 $\mu s$ pulse followed by a 40 $\mu s$ pulse
d) The exclusive-OR output is a 20 $\mu s$ pulse followed by a 15 $\mu s$ pulse, followed by a 40 $\mu s$ pulse

No, the answer is incorrect.
Score: 0
Accepted Answers: d)

10) 1 point
The carry look ahead adder is based on the principle of looking at the lower order bits of _________ and _________ if a high order carry is generated.

a) Addend, minuend
b) Minuend, subtrahend
c) Addend, minuend
d) Augend, addend

No, the answer is incorrect.
Score: 0
Accepted Answers: d)

11) 1 point
In serial addition, the addition is carried out _________

a) 3 bit per second
b) Byte by byte
c) Bit by bit
d) All bits at the same time

No, the answer is incorrect.
Score: 0
Accepted Answers: c)
12. Which statement below best describes a Karnaugh map?  
   a) It is simply a rearranged truth table  
   b) The Karnaugh map eliminates the need for using NAND and NOR gates  
   c) Variable complements can be eliminated by using Karnaugh maps  
   d) A Karnaugh map can be used to replace Boolean rules  

   No, the answer is incorrect.  
   Score: 0  
   Accepted Answers:  
   a) 

13. Each “0” entry in a K-map square represents:  
   a) A HIGH for each input truth table condition that produces a HIGH output  
   b) A HIGH output on the truth table for all LOW input combinations  
   c) A LOW output for all possible HIGH input conditions  
   d) A DON’T CARE condition for all possible input truth table combinations  

   No, the answer is incorrect.  
   Score: 0  
   Accepted Answers:  
   a) 

14. Which of the following statements accurately represents the two BEST methods of logic circuit simplification?  
   a) Actual circuit trial and error evaluation and waveform analysis  
   b) Karnaugh mapping and circuit waveform analysis  
   c) Boolean algebra and Karnaugh mapping  
   d) Boolean algebra and actual circuit trial and error evaluation  

   No, the answer is incorrect.  
   Score: 0  
   Accepted Answers:  
   c)
Looping on a K-map always results in the elimination of ________

a) Variables within the loop that appear only in their complemented form
b) Variables that remain unchanged within the loop
c) Variables within the loop that appear in both complemented and uncomplemented form
d) Variables within the loop that appear only in their uncomplemented form

No, the answer is incorrect.
Score: 0
Accepted Answers:

16) 1 point

The basic building blocks of the arithmetic unit in a digital computer are __________

a) Subtractors
b) Adders
c) Multiplexer
d) Comparator

No, the answer is incorrect.
Score: 0
Accepted Answers:

17) 1 point

Procedure for the design of combinational circuits are:
A. From the word description of the problem, identify the inputs and outputs and draw a block diagram.
B. Draw the truth table such that it completely describes the operation of the circuit for different combinations of inputs.
C. Simplify the switching expression(s) for the output(s).
D. Implement the simplified expression using logic gates.
E. Write down the switching expression(s) for the output(s).

a) B, C, D, E, A
b) A, D, E, B, C
c) A, B, E, C, D
d) B, A, E, C, D

No, the answer is incorrect.
Score: 0
Accepted Answers:
18. The design of an ALU is based on ___________
   a) Sequential logic
   b) Combinational logic
   c) Multiplexing
   d) De-Multiplexing
   
   No, the answer is incorrect.
   Score: 0
   Accepted Answers: b)

19. If the two numbers include a sign bit in the highest order position, the bit conditions of interest are the sign of the result, a zero indication and __________
   a) An underflow condition
   b) A neutral condition
   c) An overflow condition
   d) One indication
   
   No, the answer is incorrect.
   Score: 0
   Accepted Answers: c)

20. If the two numbers include a sign bit in the highest order position, the bit conditions of interest are the sign of the result, a zero indication and __________
   a) An underflow condition
   b) A neutral condition
   c) An overflow condition
   d) One indication
   
   No, the answer is incorrect.
   Score: 0
   Accepted Answers: c)

21. 

https://onlinecourses.nptel.ac.in/noc20_ee37/unit?unit=3&assessment=92
If the two numbers are unsigned, the bit conditions of interest are the ______ carry and a possible ______ result.

a) Input, zero  
b) Output, one  
c) Input, one  
d) Output, zero

No, the answer is incorrect.  
Score: 0  
Accepted Answers:  
d)

22) ______ 1 point
In a combinational circuit, the output at any time depends only on the ______ at that time.
a) Voltage  
b) Intermediate values  
c) Input values  
d) Clock pulses

No, the answer is incorrect.  
Score: 0  
Accepted Answers:  
c)

23) ______ 1 point
In a sequential circuit, the output at any time depends only on the input values at that time.
a) Past output values  
b) Intermediate values  
c) Both past output and present input  
d) Present input values

No, the answer is incorrect.  
Score: 0  
Accepted Answers:  
c)
24. Which of the following will give the sum of full adders as output?
   a) Three point major circuit
   b) Three bit parity checker
   c) Three bit comparator
   d) Three bit counter
   
   No, the answer is incorrect.
   Score: 0
   Accepted Answers:
   a)

25. Which of the following gate is known as coincidence detector?
   a) AND gate
   b) OR gate
   c) NOR gate
   d) NAND gate

   No, the answer is incorrect.
   Score: 0
   Accepted Answers:
   a)

26. The time required for a gate or inverter to change its state is called ________
   a) Rise time
   b) Decay time
   c) Propagation time
   d) Charging time

   No, the answer is incorrect.
   Score: 0
   Accepted Answers:
   c)

27)
Why is the fan-out of CMOS gates frequency dependent?

a) Each CMOS input gate has a specific propagation time and this limits the number of different gates that can be connected to the output of a CMOS gate

b) When the frequency reaches the critical value the gate will only be capable of delivering 70% of the normal output voltage and consequently the output power will be one-half of normal and this defines the upper operating frequency

c) The higher number of gates attached to the output the more frequently they will have to be serviced thus reducing the frequency at which each will be serviced with an input signal

d) The input gates of the FETs are predominantly capacitive and as the signal frequency increases the capacitive loading also increases thereby limiting the number of loads that may be attached to the output of the driving gate

○ a)
○ b)
○ c)
○ d)

No, the answer is incorrect.
Score: 0
Accepted Answers: 

d) 1 point

Logic circuits that are designated as buffers, drivers or buffers/drivers are designed to have:

a) A greater current/voltage capability than an ordinary logic circuit

b) Greater input current/voltage capability than an ordinary logic circuit

b) A smaller output current/voltage capability than an ordinary logic circuit

d) Greater the input and output current/voltage capability than an ordinary logic circuit

○ a)
○ b)
○ c)
○ d)

No, the answer is incorrect.
Score: 0
Accepted Answers: 
a) 1 point

What is the static charge that can be stored by your body as you walk across a carpet?

a) 300 volts

b) 3000 volts

c) 30000 volts

d) Over 30000 volts

○ a)
○ b)
○ c)
○ d)

No, the answer is incorrect.
Score: 0
Accepted Answers: 
d)
30) Which of the following statements apply to CMOS devices?
   a) The devices should not be inserted into circuits with the power on
   b) All tools, test equipment and metal workbenches should be tied to earth ground
   c) The devices should be stored and shipped in antistatic tubes or conductive foam
   d) All of the Mentioned

   No, the answer is incorrect.
   Score: 0
   Accepted Answers:
   d)

31) LSI means ________ and refers to ________ gates per chip.
   a) Long Scale Integration, more than 10 upto 10000
   b) Large Scale Integration, more than 100 upto 5000
   c) Large Short Integration, less than 10 and greater than 5000
   d) Long Short Integration, more than 10 upto 10000

   No, the answer is incorrect.
   Score: 0
   Accepted Answers:
   b)

32) The full form of DIP is ____________
   a) Dual-in-Long Package
   b) Dual-in-Line Package
   c) Double Integrated Package
   d) Double-in-Line Package

   No, the answer is incorrect.
   Score: 0
   Accepted Answers:
   b)