

Unit 6 - Week 4

Course outline

How does an NPTEL online course work?

Week 0

Week 1

Week 2

Week 3

Week 4

- Lecture 17: 8085 Microprocessors (Contd.)
- Lecture 18: 8085 Microprocessors (Contd.)
- Lecture 19: 8085 Microprocessors (Contd.)
- Lecture 20: 8085 Microprocessors (Contd.)
- Lecture 21: 8085 Microprocessors (Contd.)
- Week 4 : Lecture Material
- Quiz : Assignment 4**
- Week 4 Feedback Form

Week 5

Week 6

Week 7

Week 8

Week 9

Week 10

Week 11

Week 12

Download Videos

Detailed Assignment Solution

Text Transcripts

Live Interactive Session

Assignment 4

The due date for submitting this assignment has passed. **Due on 2020-02-26, 23:59 IST.**
As per our records you have not submitted this assignment.

- 1) With respect to 8085, match Column X with Column Y.
- | Column X | Column Y |
|------------|-----------------|
| 1. INTR | 1. Non-maskable |
| 2. RST 5.5 | 2. Maskable |
| 3. TRAP | 3. Software |
| 4. RST 1 | 4. Non-vectored |
- a) X1-Y2, X2-Y1, X3-Y4, X4-Y3
b) X1-Y4, X2-Y2, X3-Y1, X4-Y3
c) X1-Y3, X2-Y2, X3-Y4, X4-Y1
d) X1-Y1, X2-Y4, X3-Y2, X4-Y3
- a.
 b.
 c.
 d.
- No, the answer is incorrect.
Score: 0
Accepted Answers: b.
- 2) Interrupt vector table of 8085 ranges over
- a) 0010H-0100H
b) 0000H-FFFFH
c) 0000H-00FFH
d) 0100H-01FFH
- a.
 b.
 c.
 d.
- No, the answer is incorrect.
Score: 0
Accepted Answers: c.
- 3) The instruction RST 7 is a:
- a) Restart instruction that begins the execution of a program.
b) One-byte call to the memory address 0038H.
c) One-byte call to the memory address 0007H.
d) Hardware interrupt.
- a.
 b.
 c.
 d.
- No, the answer is incorrect.
Score: 0
Accepted Answers: b.
- 4) With respect to 8085, match Column X with Column Y.
- | Column X | Column Y |
|------------|-----------------------------|
| 1. RST 5.5 | 1. Edge-triggered |
| 2. RST 6 | 2. Level-triggered |
| 3. RST 7.5 | 3. Edge and level triggered |
| 4. RST 4.5 | 4. Software |
- a) X1-Y3, X2-Y1, X3-Y4, X4-Y2
b) X1-Y4, X2-Y2, X3-Y1, X4-Y3
c) X1-Y2, X2-Y4, X3-Y1, X4-Y3
d) X1-Y3, X2-Y4, X3-Y2, X4-Y1
- a.
 b.
 c.
 d.
- No, the answer is incorrect.
Score: 0
Accepted Answers: c.
- 5) After the execution of instruction RIM, the accumulator contained 49H. Which of the following statement is TRUE in this case?
- a) RST 5.5 is enabled and is pending.
b) RST 6.5 is enabled and is pending.
c) RST 7.5 is enabled and is pending.
d) None of the given options.
- a.
 b.
 c.
 d.
- No, the answer is incorrect.
Score: 0
Accepted Answers: c.
- 6) To which pin external DMA controller sends a control signal to an 8085 microprocessor.
- a) HOLD
b) HLDA
c) INTR
d) INTA
- a.
 b.
 c.
 d.
- No, the answer is incorrect.
Score: 0
Accepted Answers: a.
- 7) Which of the following is the correct ordering of the priority of the interrupts in 8085
- a) TRAP > RST 7.5 > RST 6.5 > RST 5.5
b) RST 7.5 > RST 6.5 > RST 5.5 > TRAP
c) TRAP > RST 5.5 > RST 6.5 > RST 7.5
d) RST 5.5 > RST 6.5 > RST 7.5 > TRAP
- a.
 b.
 c.
 d.
- No, the answer is incorrect.
Score: 0
Accepted Answers: a.
- 8) A direct memory access (DMA) transfer replies
- a) Direct transfer of data between memory and accumulator
b) Direct transfer of data between memory and I/O devices without the use of microprocessor
c) Transfer of data exclusively within microprocessor registers
d) A fast transfer of data between microprocessor and I/O devices
- a.
 b.
 c.
 d.
- No, the answer is incorrect.
Score: 0
Accepted Answers: b.
- 9) The INTR interrupt may be masked using the flag
- a) Direction flag
b) Overflow flag
c) Interrupt flag
d) Sign flag
- a.
 b.
 c.
 d.
- No, the answer is incorrect.
Score: 0
Accepted Answers: c.
- 10) At the end of ISR, the instruction should be
- a) HLT
b) RET
c) END
d) NOP
- a.
 b.
 c.
 d.
- No, the answer is incorrect.
Score: 0
Accepted Answers: b.
- 11) Which of the following statement is TRUE?
- a) In half duplex mode data transmission is one way
b) In half duplex mode data data transmission is two way
c) In full duplex mode data transmission one way
d) None of the above
- a.
 b.
 c.
 d.
- No, the answer is incorrect.
Score: 0
Accepted Answers: b.
- 12) The contents of the accumulator is AAH, after execution of SIM instruction
- a) Interrupt RST 7.5 is enabled
b) Interrupt RST 6.5 is disabled
c) Interrupt RST 6.5 is enabled
d) Transmission of serial data is enabled
- a.
 b.
 c.
 d.
- No, the answer is incorrect.
Score: 0
Accepted Answers: c.
- 13) The contents of the accumulator is BAH, after execution of SIM instruction.
- a) Reset the RST 7.5 flip-flop memory
b) Set the RST 7.5 flip-flop memory
c) Reset the RST 6.5 flip-flop memory
d) Interrupt RST 6.5 is disabled
- a.
 b.
 c.
 d.
- No, the answer is incorrect.
Score: 0
Accepted Answers: a.
- 14) What does the following set of instructions do in an 8085 microprocessor?
- ```
EI
MVI A, 08H
SIM
```
- a) Resets the 7.5 interrupt in an 8085 system.  
b) Enables all the interrupts in an 8085 system.  
c) Enables the 5.5 interrupt and masks all other interrupts in an 8085 system.  
d) Enables the 6.5 interrupt and masks all other interrupts in an 8085 system.
- a.  
 b.  
 c.  
 d.
- No, the answer is incorrect.  
Score: 0  
Accepted Answers: b.
- 15) Which of the following statement is correct:
- Statement I:** Asynchronous Serial Data transfer is used for data transfer rates  $\leq 20K$  bits/second.  
**Statement II:** Synchronous Serial Data transfer is used for data transfer rates  $\geq 20K$  bits/second.
- a) Only Statement I  
b) Only Statement II  
c) Both Statement I and II  
d) None of the above
- a.  
 b.  
 c.  
 d.
- No, the answer is incorrect.  
Score: 0  
Accepted Answers: c.