# Unit 11 - Week 9



## Assignment 9

The due date for submitting this assignment has passed.

Due on 2020-04-01, 23:59 IST.

### Assignment submitted on 2020-03-27, 07:39 IST

1) 1 point

ARM10TDMI is a

a) 3-stage pipeline processor

b) 5-stage pipeline processor

c) 6-stage pipeline processor

d) 8-stage pipeline processor

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
c.

2) 1 point

In 6 stage pipeline ARM architecture which of the following is true?

a) Both instruction and data buses are 32-bit

b) Instruction buses are 32 bits, but data buses are 64 bit

c) Instruction buses are 64 bits, but data buses are 32 bit

d) Both instruction and data buses are 64-bit

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
d.

3) 1 point

All ARM instructions are

a) 8-bit long

b) 16-bit long

c) 32-bit long

d) 64-bit long

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
c.

4) 1 point

ARM instruction set supports

a) Single load/store instructions only

b) Multiple load/store instruction that allow to load/store upto 4 registers at once

c) Multiple load/store instruction that allow to load/store upto 8 registers at once

d) Multiple load/store instruction that allow to load/store upto 16 registers at once

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
d.

5) 1 point

When a procedure call is made, the return address is automatically placed into

a) Program Counter (R15)

b) Link Register (R14)

c) Stack Pointer (R15)

d) Stack Pointer (R13)

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
b.

6) 1 point

When the processor encounters a software interrupt instruction, ARM processor enters in

a) Fast interrupt processing mode (FIQ)

b) Normal interrupt processing mode (IRQ)

c) Supervisor mode (SVC)

d) Abort mode

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
c.

7) 1 point

CPSR cannot be modified in which of the following mode?

a) Fast interrupt processing mode (FIQ)

b) Normal interrupt processing mode (IRQ)

c) User mode

d) Supervisor mode (SVC)

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
c.

8) 1 point

On reset, ARM inserts in which of the following mode?

a) Fast interrupt processing mode (FIQ)

b) Normal interrupt processing mode (IRQ)

c) Supervisor mode (SVC)

d) User mode

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
c.

9) 1 point

Which of the following ARM instructions is same as multiplying the contents of r0 by nine and storing the product in r7?

a) ADD r0, r7, r7, LSL #3

b) ADD r0, r7, r0, LSL #3

c) ADD r7, r7, r0, LSL #3

d) ADD r7, r0, r0, LSL #3

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
d.

10) 1 point

Which of the following instructions corresponds to a Multiply Accumulate instruction in ARM architecture?

a) MUL

b) UMULL

c) SMULL

d) SMLAL

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
d.

11) 1 point

Which of the following instructions corresponds to loading a signed half word in ARM architecture?

a) LDR

b) LDRS

c) LDRSH

d) LDRH

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
c.

12) 1 point

Which register is not allowed in ARM multiplication instructions?

a) R0

b) R1

c) R14

d) R15

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
d.

13) 1 point

Which algorithm used for multiplication operations in ARM processor?

a) Braun array signed multiplier

b) Booth`s algorithm for multiplication

c) Baugh wooley multiplier

d) Vedic multiplier

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
b.

14) 1 point

In which of the following modes of an ARM processor, CPSR cannot be modified?

a) Fast Interrupt Processing (FIQ) mode

b) Normal Interrupt Processing (IRQ) mode

c) User mode

d) Supervisor (SVC) mode

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
c.

15) 1 point

Which part of an ARM instruction contains one of the 16 condition codes?

a) Bit 24 to bit 21

b) Bit 31 to bit 28

c) Bit 19 to bit 16

d) Bit 15 to bit 12

a.
b.
c.
d.

No, the answer is incorrect.
Score: 0
Accepted Answers:
b.