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Courses » Optimization Techniques for Digital VLSI Design

Announcements Course Ask a Question Progress Mentor

Unit 2 - Introduction and High-level Synthesis [Part-1]

Course outline

How to access the portal

Introduction and High-level Synthesis [Part-1]

- Introduction to Digital VLSI Design Flow
- High-level Synthesis (HLS) flow with an example
- Automation of High-level Synthesis Steps
- Quiz : Assignment for Week 1
- Solution of Assignment 1

Introduction and High-level Synthesis [Part-2]

RTL Optimizations [Part-1]

RTL Optimizations [Part-2]

Logic Synthesis and Physical Synthesis

VLSI Testing [Part-1]

VLSI Testing [Part-2]

Assignment for Week 1

The due date for submitting this assignment has passed. **Due on 2018-02-21, 23:59 IST.**

Submitted assignment

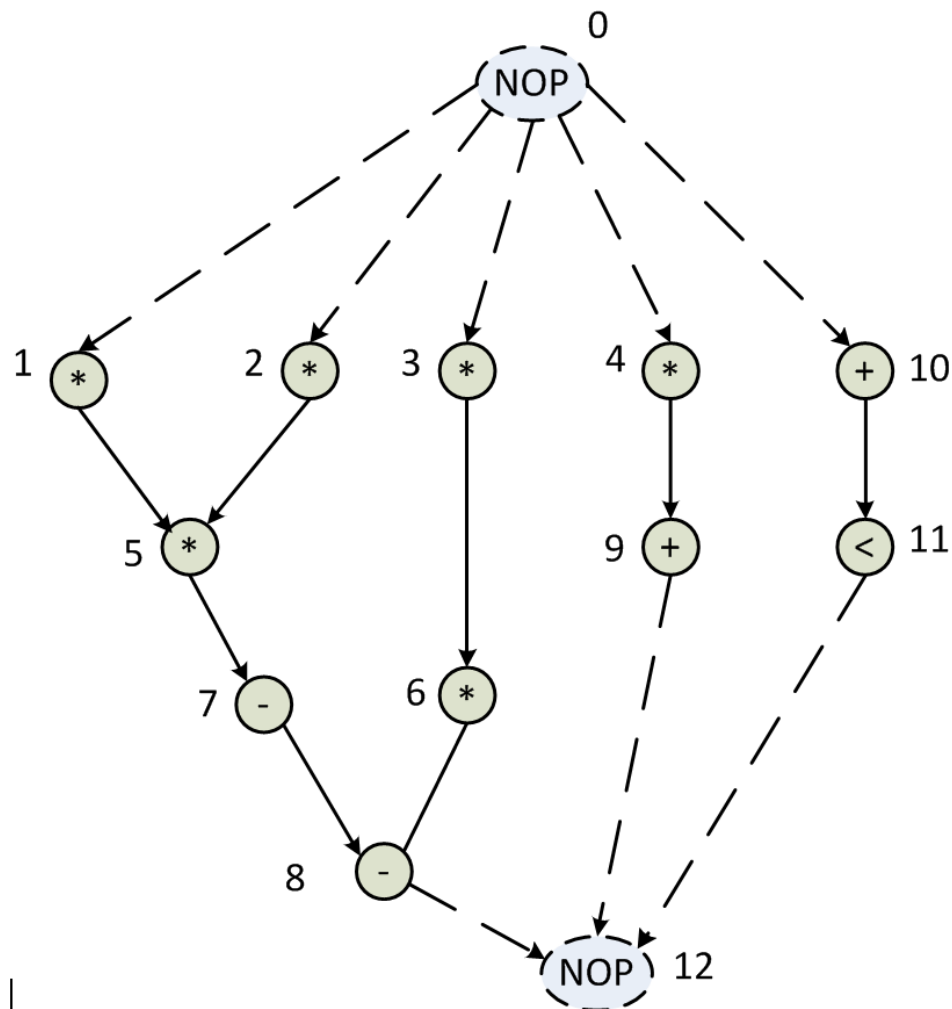


Figure-1

1) To calculate the output of the expression "3 * 5 * (5 + 6)", which one is the following is an invalid sequence of operations. **1 point**

- t1 = 3 * 5; t3 = t1 * t2; t2 = 5 + 6
- t1 = 3 * 5; t2 = 5 + 6; t3 = t1 * t2
- t2 = 5 + 6; t1 = 3 * 5; t3 = t1 * t2

Verification [Part-1]

Verification [Part-2]

None of above.

No, the answer is incorrect.

Score: 0

Accepted Answers:

$t1 = 3 * 5; t3 = t1 * t2; t2 = 5 + 6$

2) You are given sufficient number of resources where all operations except node 0 and 12 take **1 point** 1 time step (node 0 and 12 takes 0 time step). Find minimum number of time steps required to schedule the sequence graph shown in figure-1?

- 2
 4
 3
 5

No, the answer is incorrect.

Score: 0

Accepted Answers:

4

3) You are given **2 Multipliers, 1 Adder / Subtraction unit** and **1 Comparator**. What will be **1 point** the minimum number of time steps required for the graph in figure-1, where assumptions are same as question 2.

- 4
 5
 6
 7

No, the answer is incorrect.

Score: 0

Accepted Answers:

5

4) What will be the ASAP schedule time step of nodes 1, 7 and 9 of figure-1 each operation **1 point** takes 1 time step to execute.

- 1, 3, 3
 1, 3, 2
 1, 3, 4
 1, 4, 3

No, the answer is incorrect.

Score: 0

Accepted Answers:

1, 3, 2

5) What will be the ALAP time of nodes 1, 7 and 9 of figure-1 with given latency bound is 5 and **1 point** each operation takes 1 time step to execute.

- 2, 4, 4
 2, 3, 4
 2, 4, 5
 None of above

No, the answer is incorrect.

Score: 0

Accepted Answers:

2, 4, 5

6) What will be mobility of node 1, 7 and 9 considering the ASAP and ALAP scheduling of **1 point** questions 4 and 5?

- 1, 1, 3

- 1, 0, 2
- 0, 1, 3
- 1, 0, 3

No, the answer is incorrect.

Score: 0

Accepted Answers:

1, 1, 3

7) Suppose, multiplication operation takes 2 time steps and all other operation takes 1 time step. Also, there is not resource bound. What will be minimum latency of the graph in figure-1? **1 point**

- 3
- 4
- 5
- 6

No, the answer is incorrect.

Score: 0

Accepted Answers:

6

8) Consider the Integer Linear Programming (ILP) formulation of Minimum-Latency Scheduling under Resource Constraints (ML-RC). Which of the following constraints must be satisfied in ML-RC formulation. **1 point**

S1: Start time of each operation must be unique

S2: Precedence relationships must be satisfied

S3: Resource constraints must be met

- S1, S2
- S1, S3
- S2, S3
- S1, S2, S3

No, the answer is incorrect.

Score: 0

Accepted Answers:

S1, S2, S3

9) Which of the following statements are true about allocation and binding phase of high-level synthesis? **1 point**

S1: Same adder can be used to execute two addition operations if these two addition operations are scheduled in the same time step.

S2: Same adder can be used to execute two addition operations if these two addition operations are scheduled in different time step.

- S1
- S2
- S1 and S2
- None

No, the answer is incorrect.

Score: 0

Accepted Answers:

S2

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