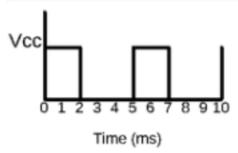
Unit 12 - Week 10

Assignment 10

The due date for submitting this assignment has passed.
As per our records you have not submitted this assignment.

Due on 2020-11-25, 23:59 IST.

1) What is the duty cycle of the following waveform? *1 point*



- 75%
- 60%
- 50%
- 40%

No, the answer is incorrect.
Score: 0
Accepted Answers:
40%

2) For a given clock signal, what is the relation between frequency and resolution of the PWM signal? *1 point*

- Higher the frequency of PWM signal, higher the resolution
- Lower the frequency of PWM signal, higher the resolution
- There is no relation
- None of the above

No, the answer is incorrect.
Score: 0
Accepted Answers:
Lower the frequency of PWM signal, higher the resolution

3) Find the frequency and resolution of PWM generated using TimerA0 in MSP430: TACCR0 = 255, TACCR1 = 64, timer clock frequency = 1MHz *1 point*

- Frequency = 16 KHz, resolution = 1/256
- Frequency = 16 KHz, resolution = 1/64
- Frequency = 4 KHz, resolution = 1/256
- Frequency = 4 KHz , resolution = 1/64

No, the answer is incorrect.
Score: 0
Accepted Answers:
Frequency = 4 KHz, resolution = 1/256

4) Which Timer mode is used to generate PWM? *1 point*

- Capture mode
- Compare mode
- Both a and b
- Continuous Mode

No, the answer is incorrect.
Score: 0
Accepted Answers:
Compare mode

5) What happens in output mode 7 (on TA0.1 output pin)? *1 point*

- The output is reset when TAR = TACCR0 and set when TAR = TACCR1
- The output is set when TAR = TACCR0 and reset when TAR = TACCR1.
- The output is reset when TAR = TACCR0 and toggled when TAR = TACCR1
- The output is toggled when TAR = TACCR0 and set when TAR = TACCR1

No, the answer is incorrect.
Score: 0
Accepted Answers:
The output is set when TAR = TACCR0 and reset when TAR = TACCR1.

6) Which analog to digital converter is considered to be the fastest among the following options? *1 point*

- Counter Type ADC
- SAR type ADC
- Dual Slope ADC
- Flash Type ADC

No, the answer is incorrect.
Score: 0
Accepted Answers:
Flash Type ADC

7) In a SAR type A/D converter, if the clock period is 1us and the resolution is 10 bits then calculate the maximum rate at which the A/D converter can work *1 point*

- 1000000 samples/sec
- 100000 samples/sec
- 10000 samples/sec
- 1024 samples/sec

No, the answer is incorrect.
Score: 0
Accepted Answers:
100000 samples/sec

8) In a 10 bit A/D converter having an input range of 3.3V, what would be the correct digital representation of the voltage 3V? *1 point*

- 1110110101
- 1110110100
- 1110100010
- 1110100011

No, the answer is incorrect.
Score: 0
Accepted Answers:
1110100010

9) A 4 bit input D/A converter is made up of resistor divider ('0'=0V, '1'=10V), then the analog voltage for a digital value of input 1101 is *1 point*

- 7(1/3) V
- 13 V
- 8.125 V
- 7.5 V

No, the answer is incorrect.
Score: 0
Accepted Answers:
8.125 V

10) What is/are the major advantage of the R/2R ladder D/A converter as compared to a binary weighted D/A converter *1 point*

- It only uses two values of resistors
- Its operation is much easier to analyze
- It has fewer parts for the same number of inputs
- All of the above

No, the answer is incorrect.
Score: 0
Accepted Answers:
It only uses two values of resistors